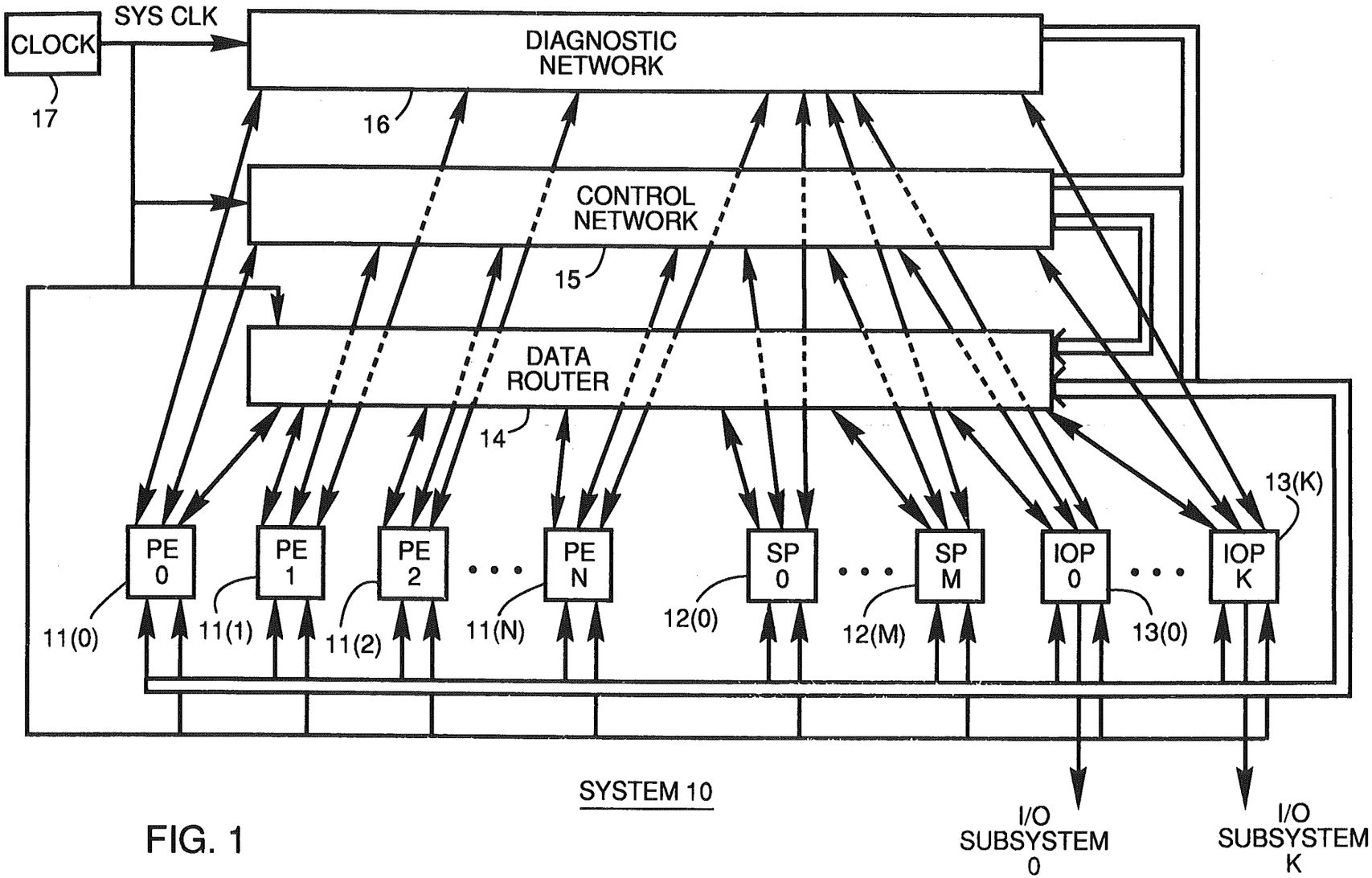
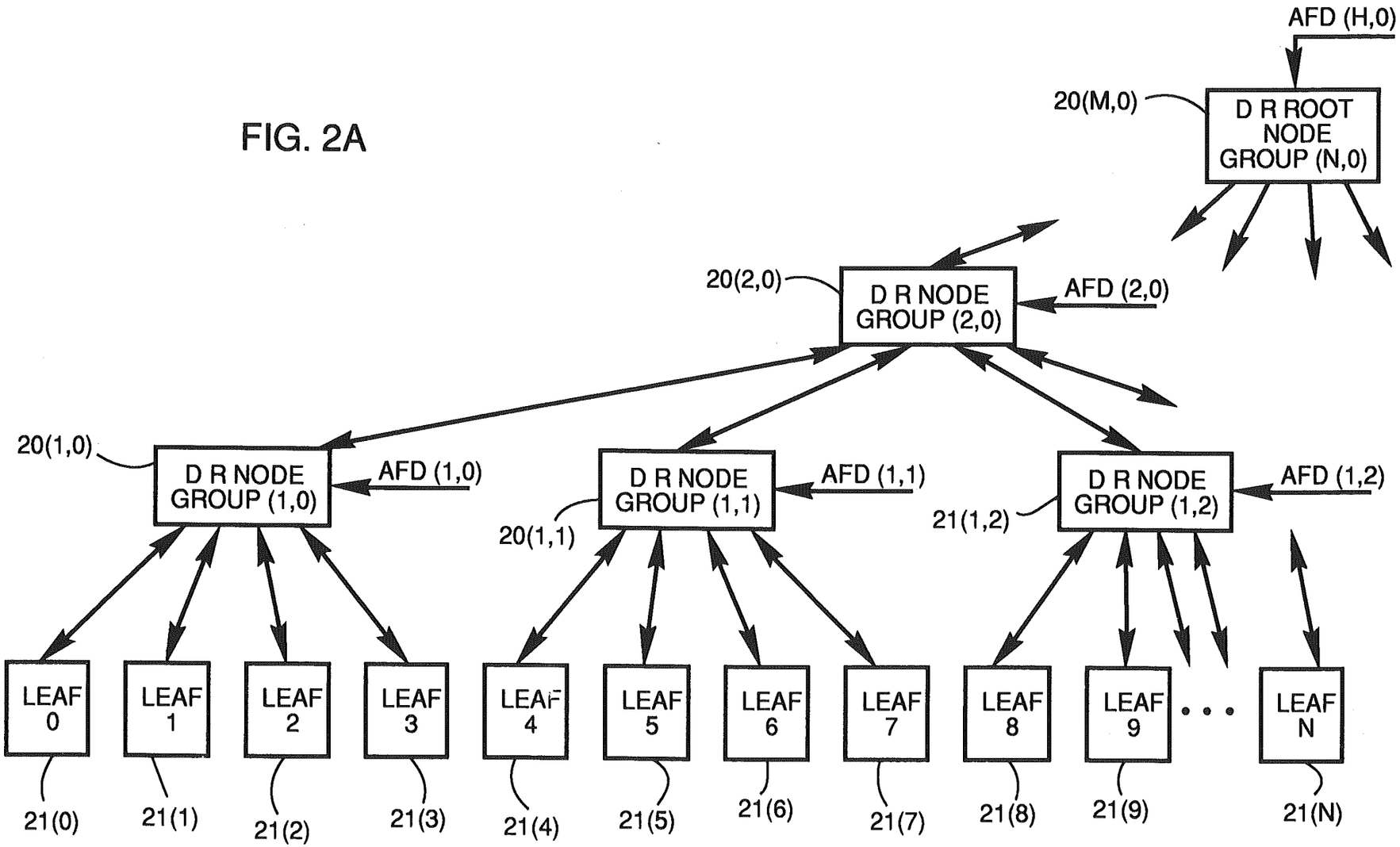

CLOCK
SYS CLK
17
DIAGNOSTIC NETWORK
16
CONTROL NETWORK
15
DATA ROUTER
14
PE 0
PE 1
PE 2
PE N
SP 0
SP M
IOP 0
IOP K
13(K)
11(0)
11(1)
11(2)
11(N)
12(0)
12(M)
13(0)
SYSTEM 10
I/O SUBSYSTEM 0
I/O SUBSYSTEM K

FIG. 1

FIG. 2A


AFD (H,0)
20(M,0)
D R ROOT NODE GROUP (N,0)
20(2,0)
D R NODE GROUP (2,0)
AFD (2,0)
20(1,0)
D R NODE GROUP (1,0)
AFD (1,0)
20(1,1)
D R NODE GROUP (1,1)
AFD (1,1)
21(1,2)
D R NODE GROUP (1,2)
AFD (1,2)
LEAF 0
LEAF 1
LEAF 2
LEAF 3
LEAF 4
LEAF 5
LEAF 6
LEAF 7
LEAF 8
LEAF 9
LEAF N
21(0)
21(1)
21(2)
21(3)
21(4)
21(5)
21(6)
21(7)
21(8)
21(9)
21(N)

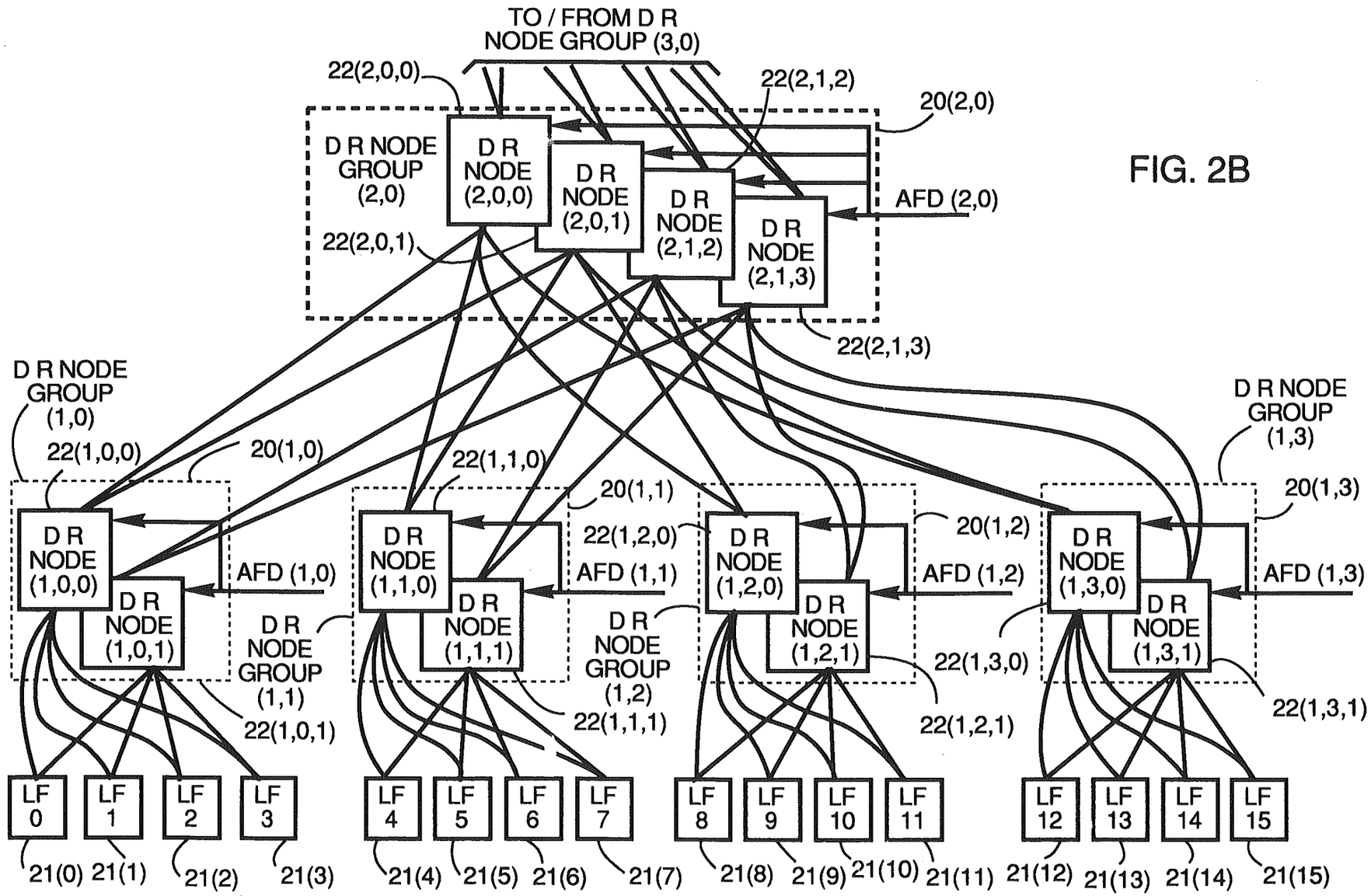

TO / FROM D R NODE GROUP (3,0)
22(2,0,0)
22(2,1,2)
20(2,0)
D R NODE GROUP (2,0)
D R NODE (2,0,0)
D R NODE (2,0,1)
D R NODE (2,1,2)
D R NODE (2,1,3)
AFD (2,0)
22(2,0,1)
22(2,1,3)
D R NODE GROUP (1,0)
22(1,0,0)
20(1,0)
22(1,1,0)
20(1,1)
22(1,2,0)
20(1,2)
D R NODE GROUP (1,3)
20(1,3)
D R NODE (1,0,0)
D R NODE (1,0,1)
AFD (1,0)
D R NODE GROUP (1,1)
22(1,0,1)
D R NODE (1,1,0)
D R NODE (1,1,1)
AFD (1,1)
D R NODE GROUP (1,2)
22(1,1,1)
D R NODE (1,2,0)
D R NODE (1,2,1)
AFD (1,2)
22(1,2,1)
D R NODE (1,3,0)
D R NODE (1,3,1)
AFD (1,3)
22(1,3,0)
22(1,3,1)
LF 0
LF 1
LF 2
LF 3
LF 4
LF 5
LF 6
LF 7
LF 8
LF 9
LF 10
LF 11
LF 12
LF 13
LF 14
LF 15
21(0)
21(1)
21(2)
21(3)
21(4)
21(5)
21(6)
21(7)
21(8)
21(9)
21(10)
21(11)
21(12)
21(13)
21(14)
21(15)

FIG. 2B

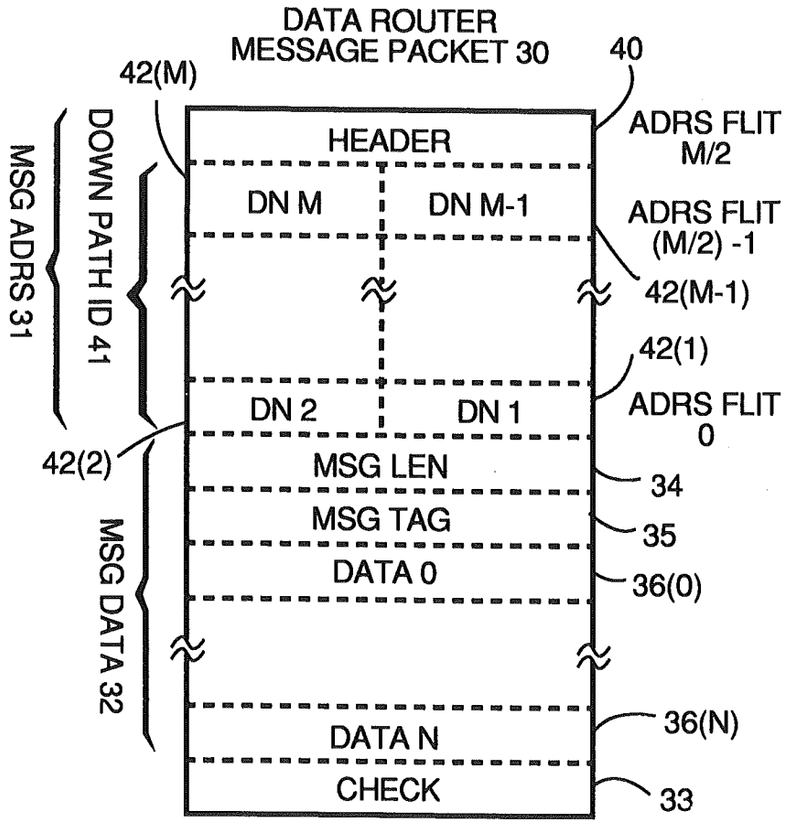

DATA ROUTER
MESSAGE PACKET 30
42(M)
40
ADRS FLIT
M/2
HEADER
DN M
DN M-1
ADRS FLIT
(M/2) -1
42(M-1)
42(1)
ADRS FLIT
0
DN 2
DN 1
MSG ADRS 31
DOWN PATH ID 41
42(2)
MSG LEN
34
MSG TAG
35
DATA 0
36(0)
MSG DATA 32
DATA N
36(N)
CHECK
33

FIG. 3

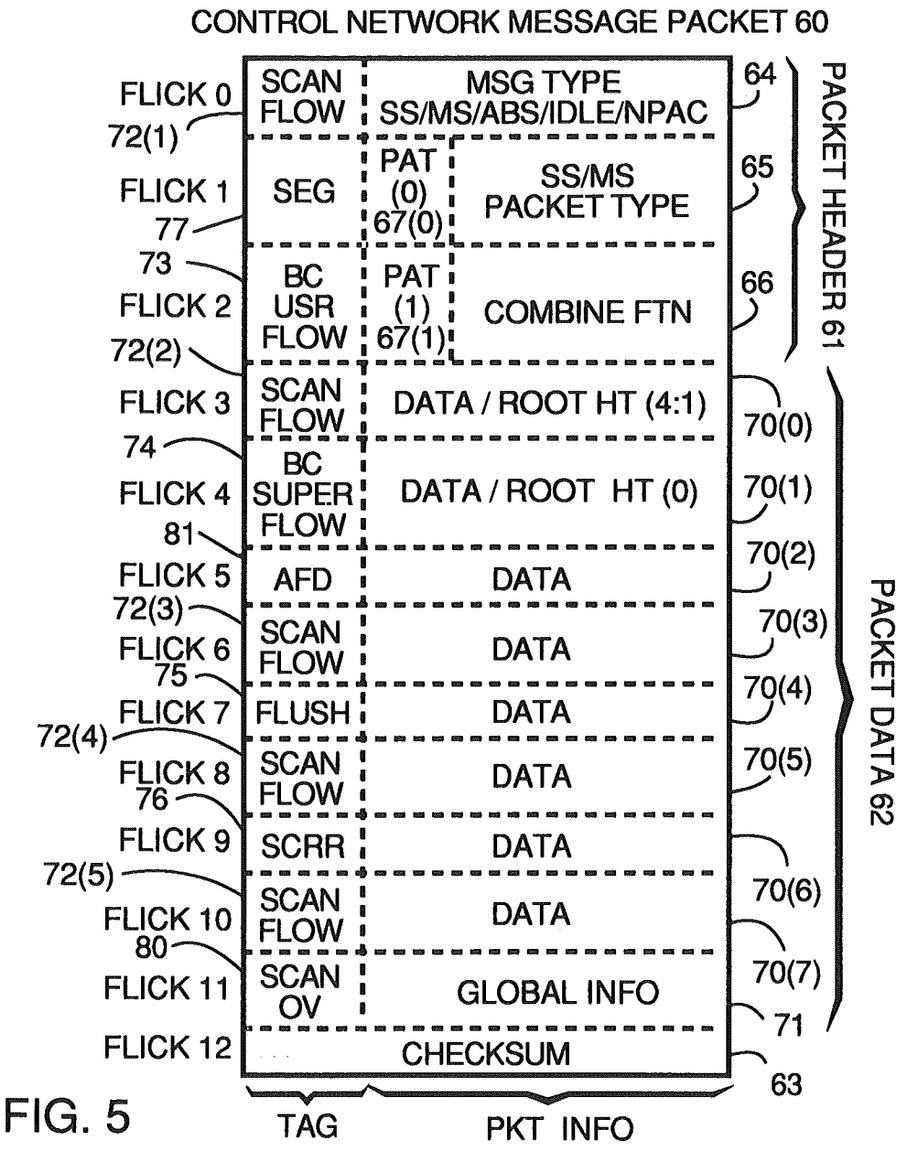
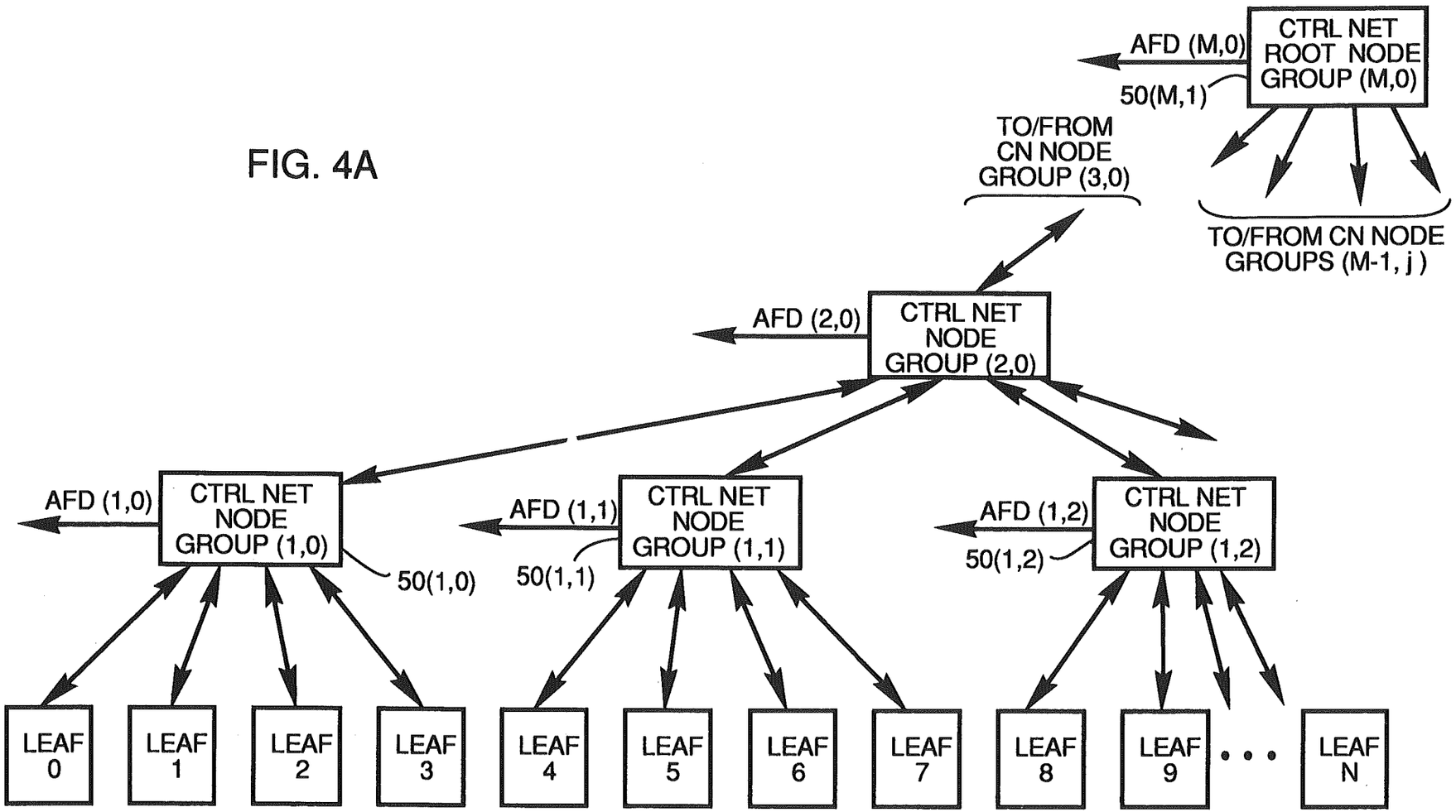

CONTROL NETWORK MESSAGE PACKET 60
FLICK 0
72(1)
SCAN FLOW
MSG TYPE
SS/MS/ABS/IDLE/NPAC
64
PACKET HEADER 61
FLICK 1
77
SEG
PAT (0) 67(0)
SS/MS PACKET TYPE
65
73
FLICK 2
72(2)
BC USR FLOW
PAT (1) 67(1)
COMBINE FTN
66
FLICK 3
SCAN FLOW
DATA / ROOT HT (4:1)
70(0)
74
FLICK 4
BC SUPER FLOW
DATA / ROOT HT (0)
70(1)
81
FLICK 5
AFD
DATA
70(2)
72(3)
FLICK 6
SCAN FLOW
DATA
70(3)
75
FLICK 7
FLUSH
DATA
70(4)
72(4)
FLICK 8
SCAN FLOW
DATA
70(5)
76
FLICK 9
SCRR
DATA
72(5)
FLICK 10
SCAN FLOW
DATA
70(6)
80
FLICK 11
SCAN OV
GLOBAL INFO
70(7)
71
FLICK 12
CHECKSUM
63
PACKET DATA 62
TAG
PKT INFO

FIG. 5

FIG. 4A


CTRL NET ROOT NODE GROUP (M,0)
AFD (M,0)
50(M,1)
TO/FROM CN NODE GROUP (3,0)
TO/FROM CN NODE GROUPS (M-1, j)
CTRL NET NODE GROUP (2,0)
AFD (2,0)
CTRL NET NODE GROUP (1,0)
AFD (1,0)
50(1,0)
CTRL NET NODE GROUP (1,1)
AFD (1,1)
50(1,1)
CTRL NET NODE GROUP (1,2)
AFD (1,2)
50(1,2)
LEAF 0
LEAF 1
LEAF 2
LEAF 3
LEAF 4
LEAF 5
LEAF 6
LEAF 7
LEAF 8
LEAF 9
LEAF N

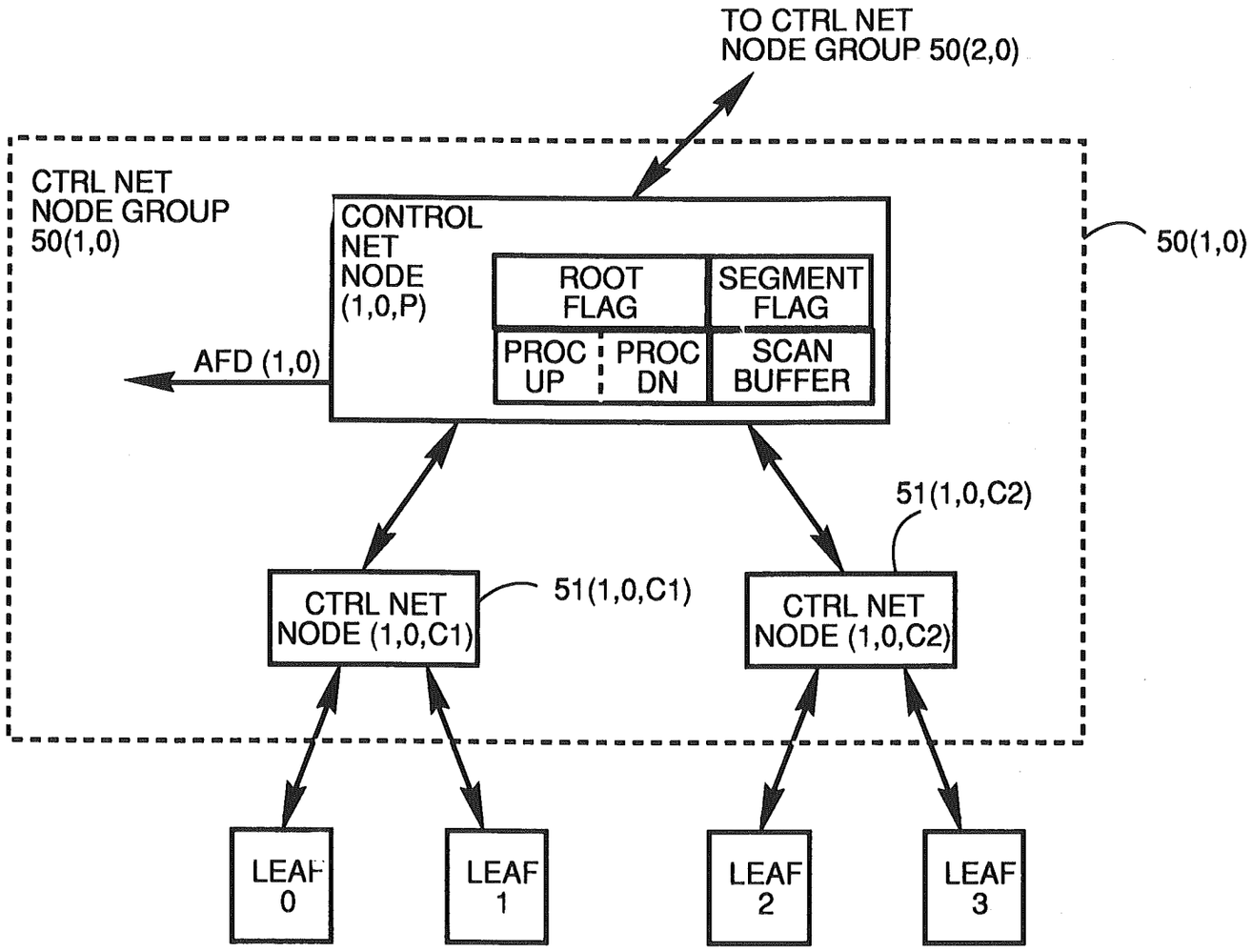

TO CTRL NET
NODE GROUP 50(2,0)
CTRL NET
NODE GROUP
50(1,0)
CONTROL
NET
NODE
(1,0,P)
ROOT
FLAG
SEGMENT
FLAG
PROC
UP
PROC
DN
SCAN
BUFFER
AFD (1,0)
50(1,0)
51(1,0,C2)
CTRL NET
NODE (1,0,C1)
51(1,0,C1)
CTRL NET
NODE (1,0,C2)
LEAF
0
LEAF
1
LEAF
2
LEAF
3

FIG. 4B

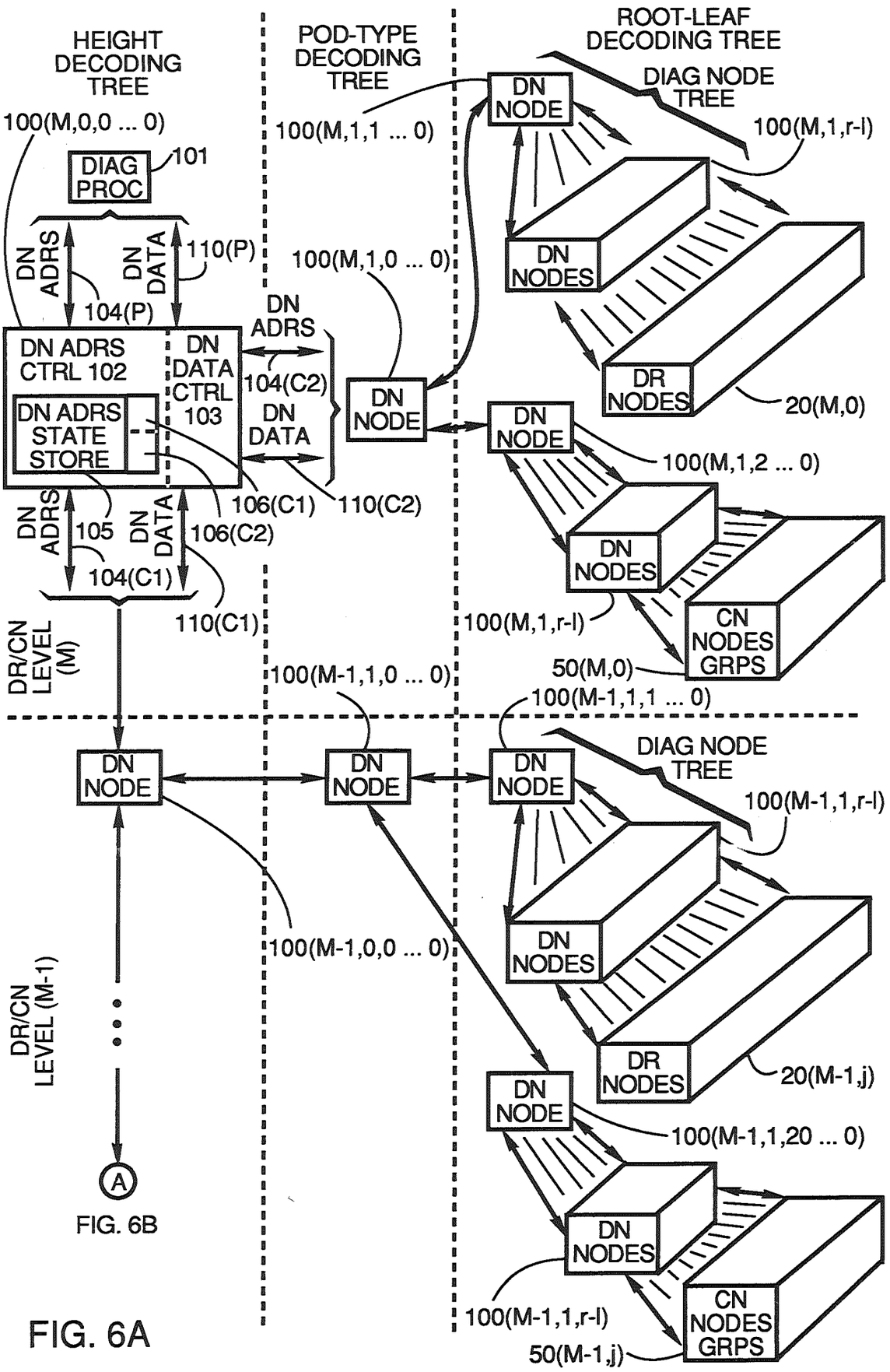

HEIGHT DECODING TREE
POD-TYPE DECODING TREE
ROOT-LEAF DECODING TREE
DIAG NODE TREE
100(M,0,0 ... 0)
DIAG PROC
101
DN ADRS
DN DATA
110(P)
104(P)
100(M,1,1 ... 0)
DN NODE
100(M,1,r-l)
DN NODES
100(M,1,0 ... 0)
DN ADRS CTRL 102
DN DATA CTRL 103
DN ADRS STATE STORE
104(C2)
DN DATA
DR NODES
20(M,0)
106(C1)
110(C2)
100(M,1,2 ... 0)
105
106(C2)
104(C1)
110(C1)
CN NODES GRPS
100(M,1,r-l)
50(M,0)
DR/CN LEVEL (M)
100(M-1,1,0 ... 0)
100(M-1,1,1 ... 0)
DIAG NODE TREE
100(M-1,1,r-l)
100(M-1,0,0 ... 0)
20(M-1,j)
DR/CN LEVEL (M-1)
100(M-1,1,20 ... 0)
A
100(M-1,1,r-l)
50(M-1,j)

FIG. 6B

FIG. 6A

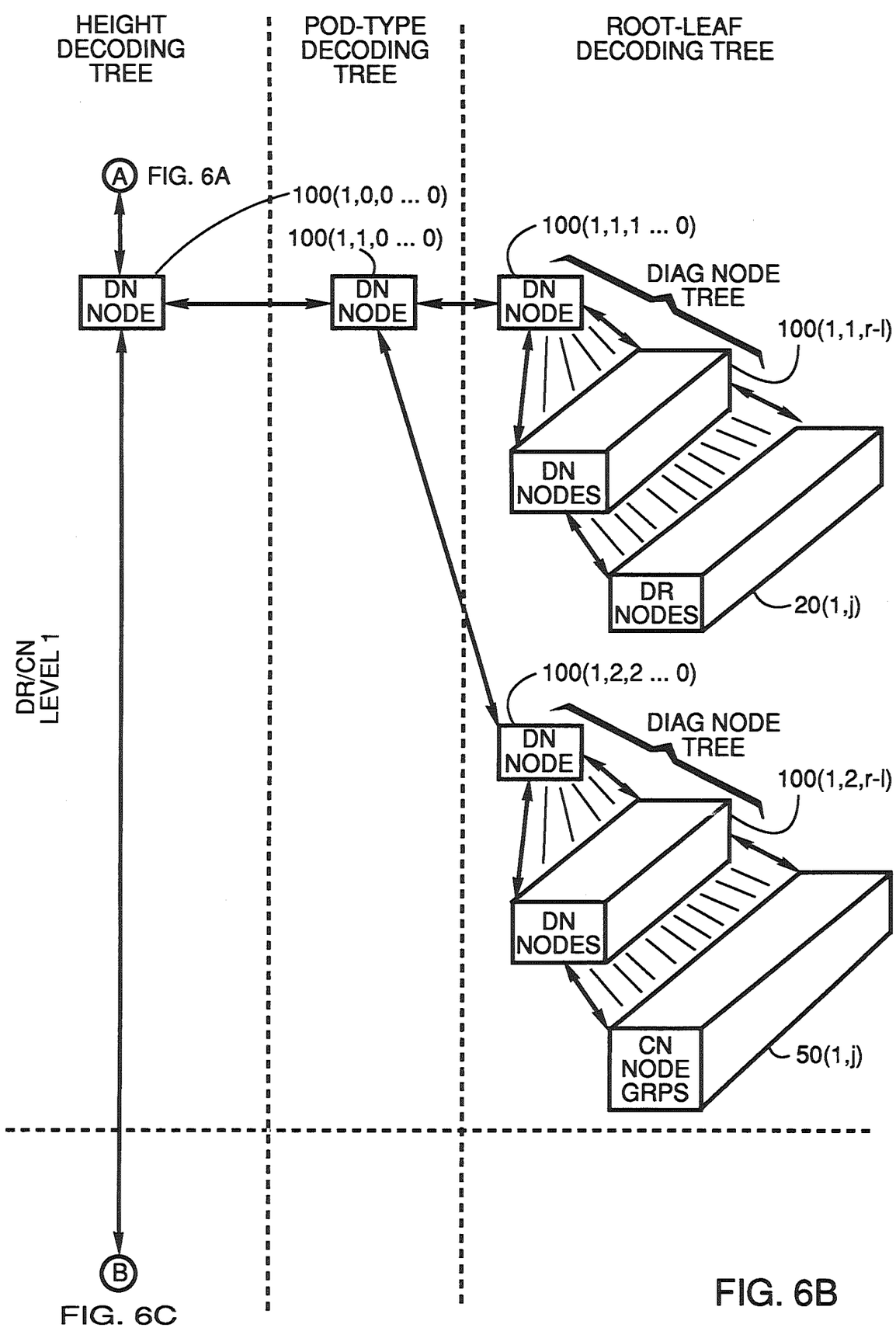

HEIGHT DECODING TREE
POD-TYPE DECODING TREE
ROOT-LEAF DECODING TREE
A
FIG. 6A
100(1,0,0 ... 0)
100(1,1,0 ... 0)
100(1,1,1 ... 0)
DN NODE
DN NODE
DN NODE
DIAG NODE TREE
100(1,1,r-l)
DN NODES
DR NODES
20(1,j)
DR/CN LEVEL 1
100(1,2,2 ... 0)
DN NODE
DIAG NODE TREE
100(1,2,r-l)
DN NODES
CN NODE GRPS
50(1,j)
B
FIG. 6C

FIG. 6B

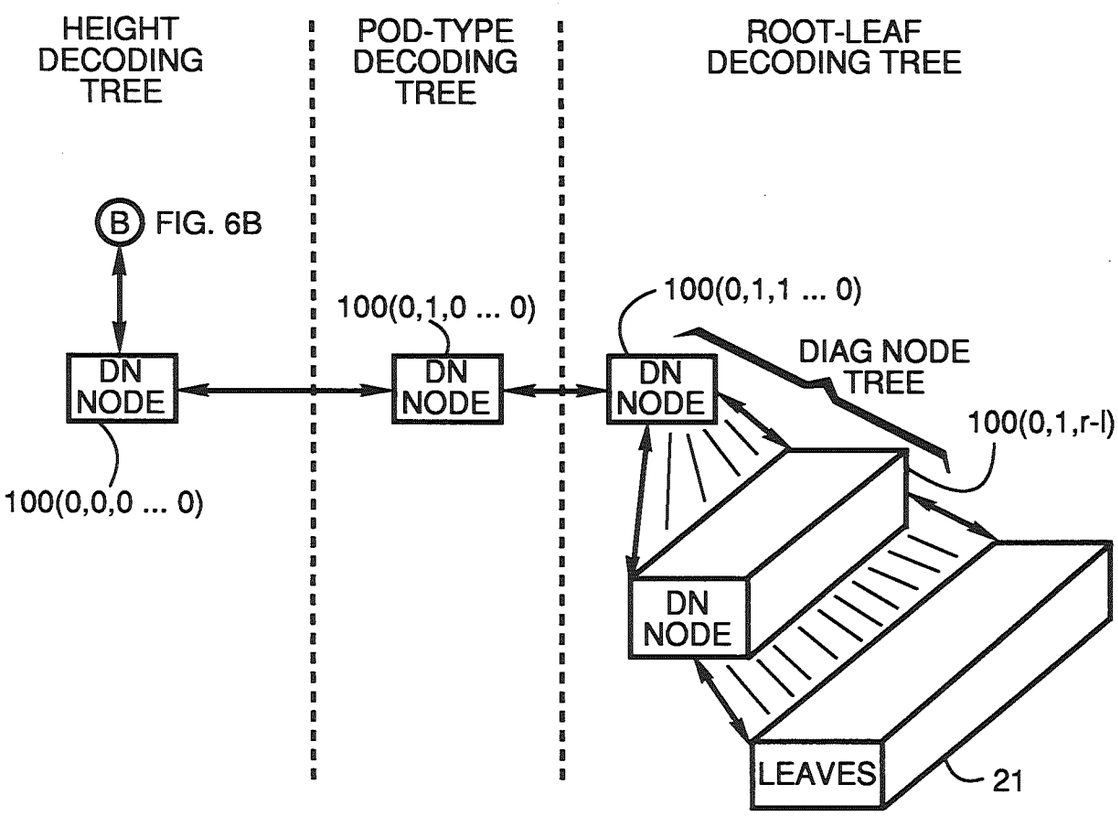

HEIGHT DECODING TREE
POD-TYPE DECODING TREE
ROOT-LEAF DECODING TREE
B
FIG. 6B
100(0,1,0 ... 0)
100(0,1,1 ... 0)
DIAG NODE TREE
DN NODE
DN NODE
DN NODE
100(0,1,r-l)
100(0,0,0 ... 0)
DN NODE
LEAVES
21

FIG. 6C

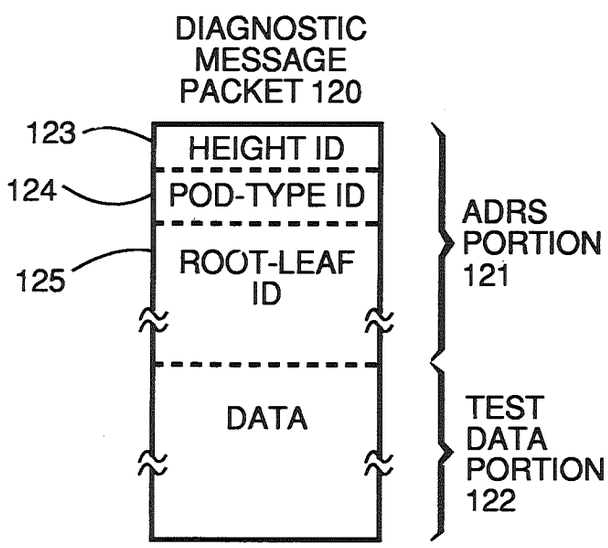

DIAGNOSTIC MESSAGE PACKET 120
123
HEIGHT ID
124
POD-TYPE ID
125
ROOT-LEAF ID
ADRS PORTION 121
DATA
TEST DATA PORTION 122

FIG. 7

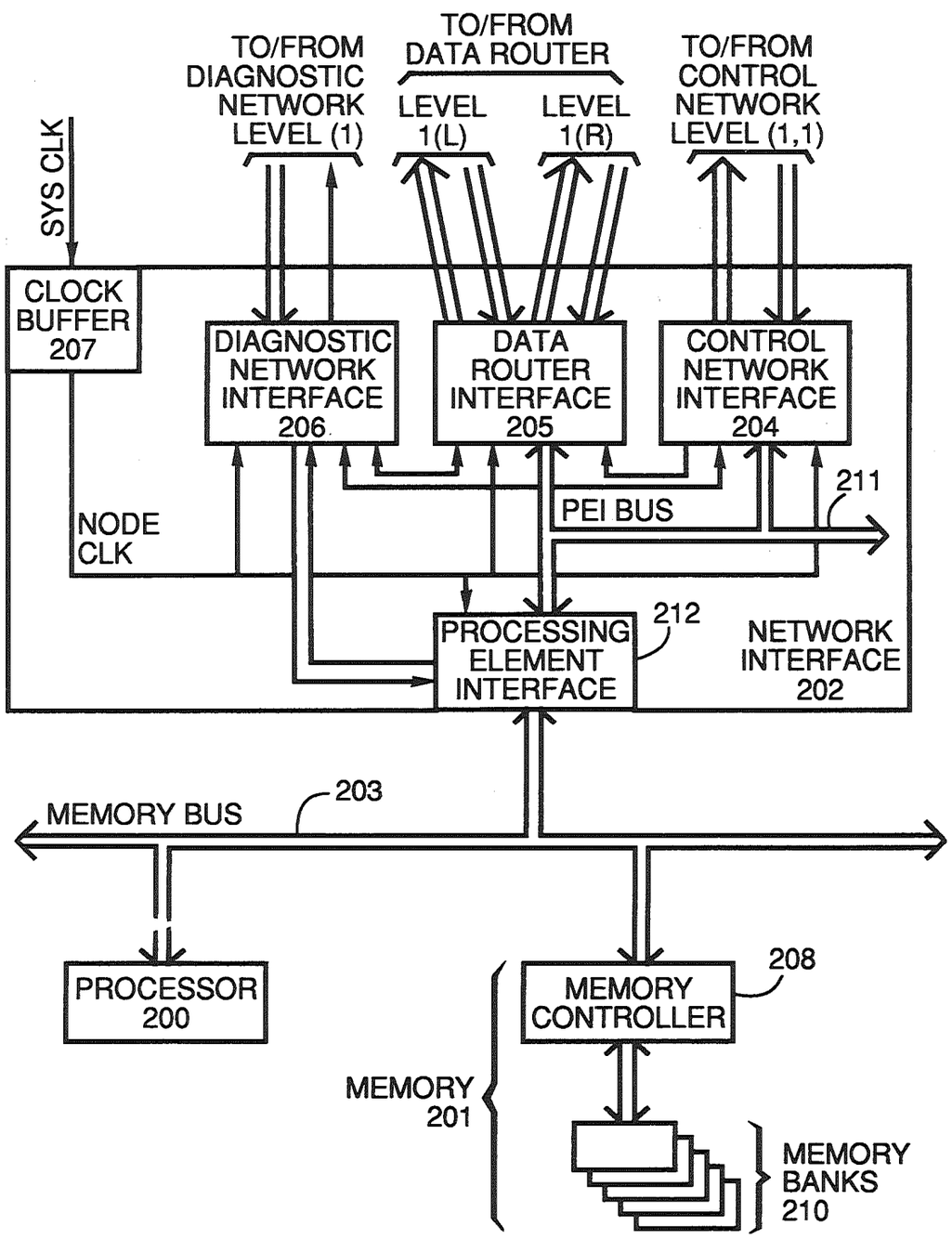

TO/FROM DIAGNOSTIC NETWORK LEVEL (1)
TO/FROM DATA ROUTER
LEVEL 1(L)
LEVEL 1(R)
TO/FROM CONTROL NETWORK LEVEL (1,1)
SYS CLK
CLOCK BUFFER 207
DIAGNOSTIC NETWORK INTERFACE 206
DATA ROUTER INTERFACE 205
CONTROL NETWORK INTERFACE 204
211
PEI BUS
NODE CLK
212
PROCESSING ELEMENT INTERFACE
NETWORK INTERFACE 202
203
MEMORY BUS
PROCESSOR 200
208
MEMORY CONTROLLER
MEMORY 201
MEMORY BANKS 210

FIG. 8

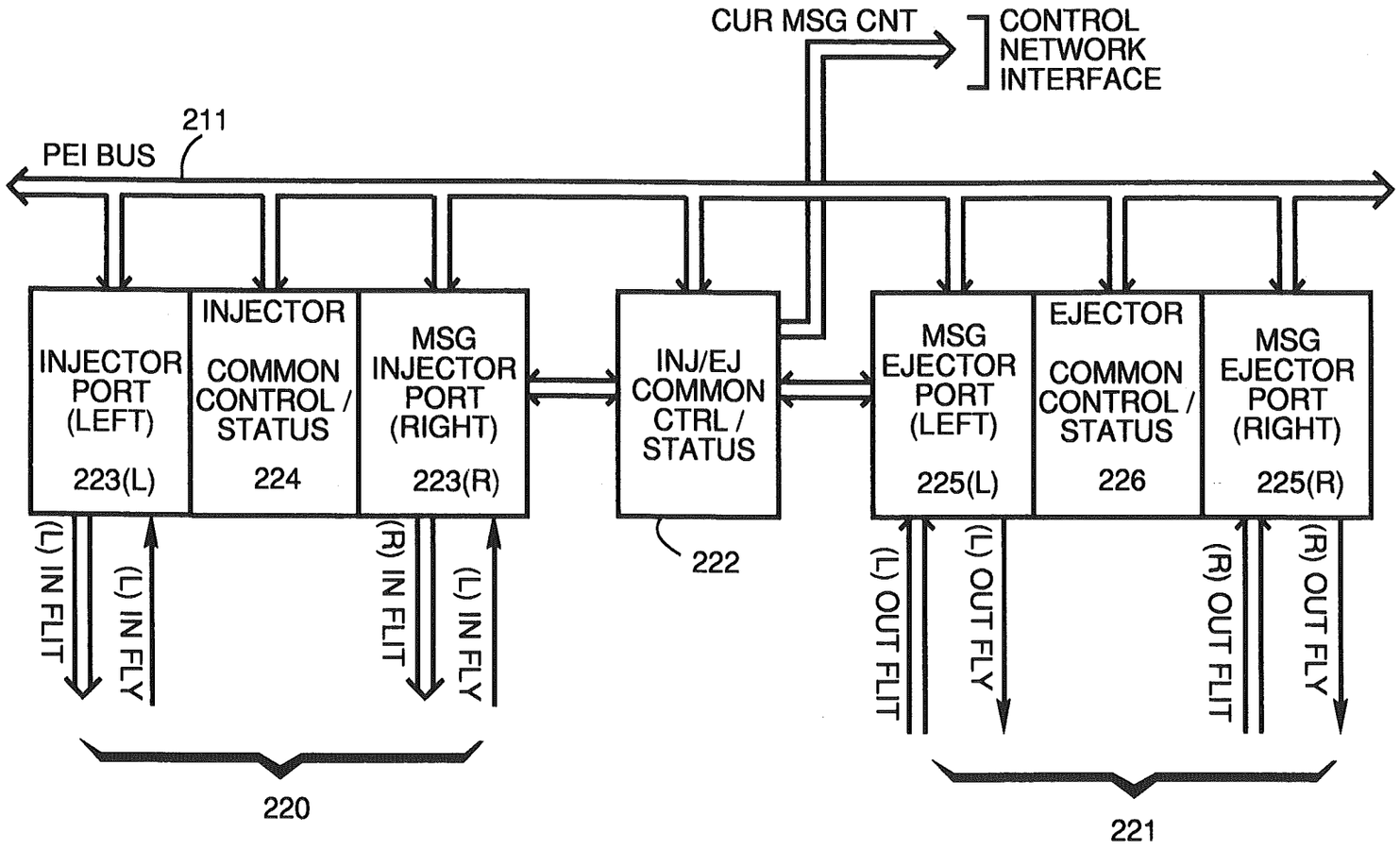

CUR MSG CNT
CONTROL NETWORK INTERFACE
211
PEI BUS
INJECTOR PORT (LEFT) 223(L)
INJECTOR COMMON CONTROL / STATUS 224
MSG INJECTOR PORT (RIGHT) 223(R)
INJ/EJ COMMON CTRL / STATUS
222
MSG EJECTOR PORT (LEFT) 225(L)
EJECTOR COMMON CONTROL / STATUS 226
MSG EJECTOR PORT (RIGHT) 225(R)
(L) IN FLIT
(L) IN FLY
(R) IN FLIT
(L) IN FLY
(L) OUT FLIT
(L) OUT FLY
(R) OUT FLIT
(R) OUT FLY
220
221

FIG. 9A-1

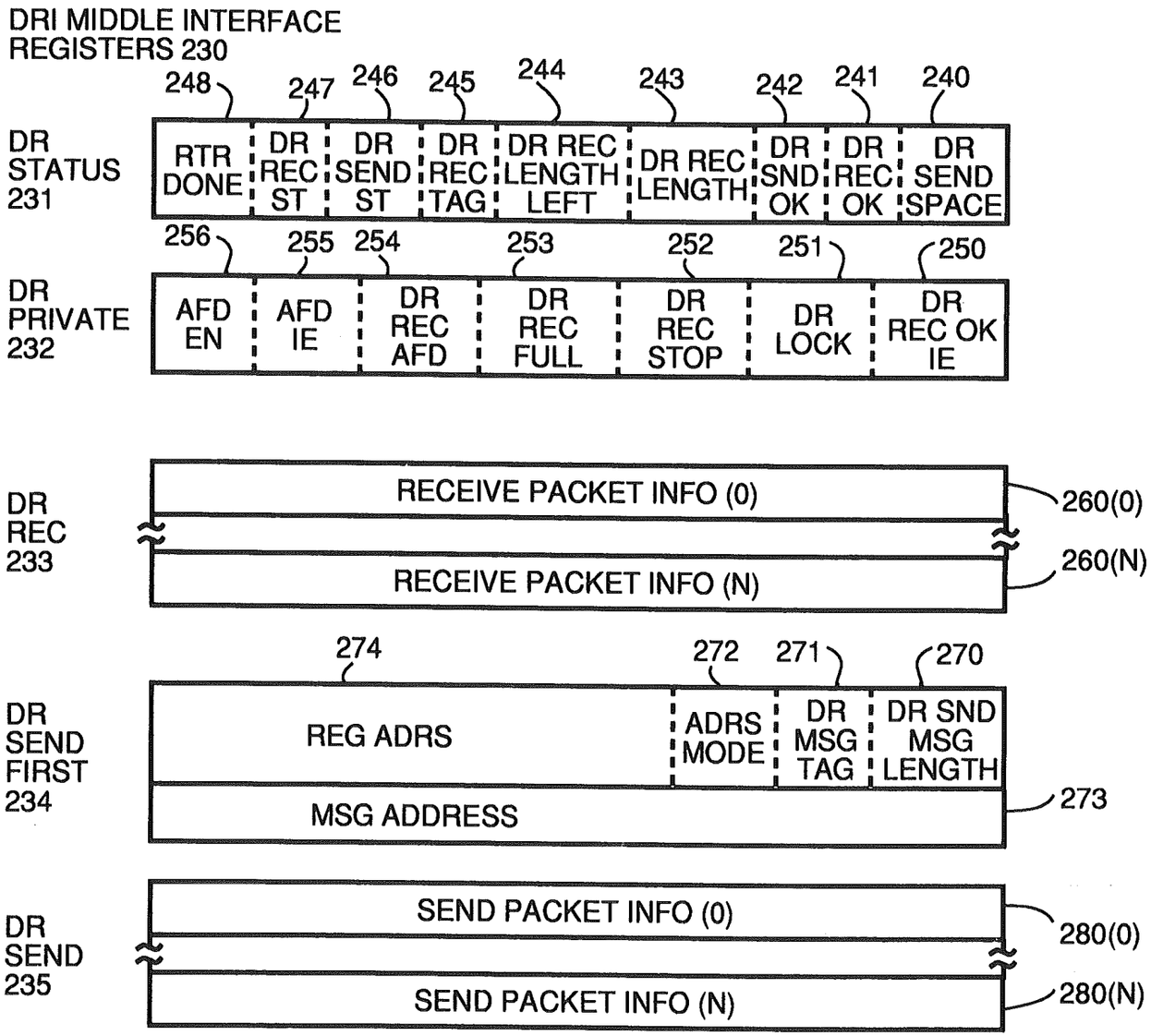

DRI MIDDLE INTERFACE REGISTERS 230
DR STATUS 231
248
247
246
245
244
243
242
241
240
RTR DONE
DR REC ST
DR SEND ST
DR REC TAG
DR REC LENGTH LEFT
DR REC LENGTH
DR SND OK
DR REC OK
DR SEND SPACE
DR PRIVATE 232
256
255
254
253
252
251
250
AFD EN
AFD IE
DR REC AFD
DR REC FULL
DR REC STOP
DR LOCK
DR REC OK IE
DR REC 233
RECEIVE PACKET INFO (0)
260(0)
RECEIVE PACKET INFO (N)
260(N)
DR SEND FIRST 234
274
272
271
270
REG ADRS
ADRS MODE
DR MSG TAG
DR SND MSG LENGTH
MSG ADDRESS
273
DR SEND 235
SEND PACKET INFO (0)
280(0)
SEND PACKET INFO (N)
280(N)

FIG. 9A-2A

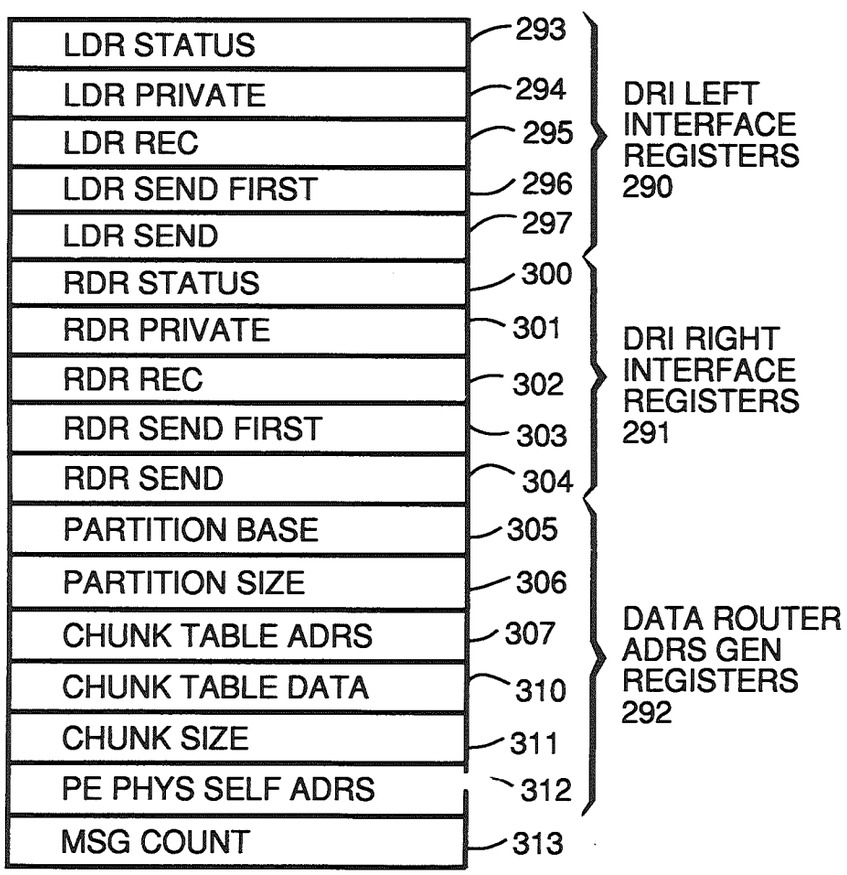

LDR STATUS
LDR PRIVATE
LDR REC
LDR SEND FIRST
LDR SEND
RDR STATUS
RDR PRIVATE
RDR REC
RDR SEND FIRST
RDR SEND
PARTITION BASE
PARTITION SIZE
CHUNK TABLE ADRS
CHUNK TABLE DATA
CHUNK SIZE
PE PHYS SELF ADRS
MSG COUNT
293
294
295
296
297
300
301
302
303
304
305
306
307
310
311
312
313
DRI LEFT INTERFACE REGISTERS 290
DRI RIGHT INTERFACE REGISTERS 291
DATA ROUTER ADRS GEN REGISTERS 292

FIG. 9A-2B

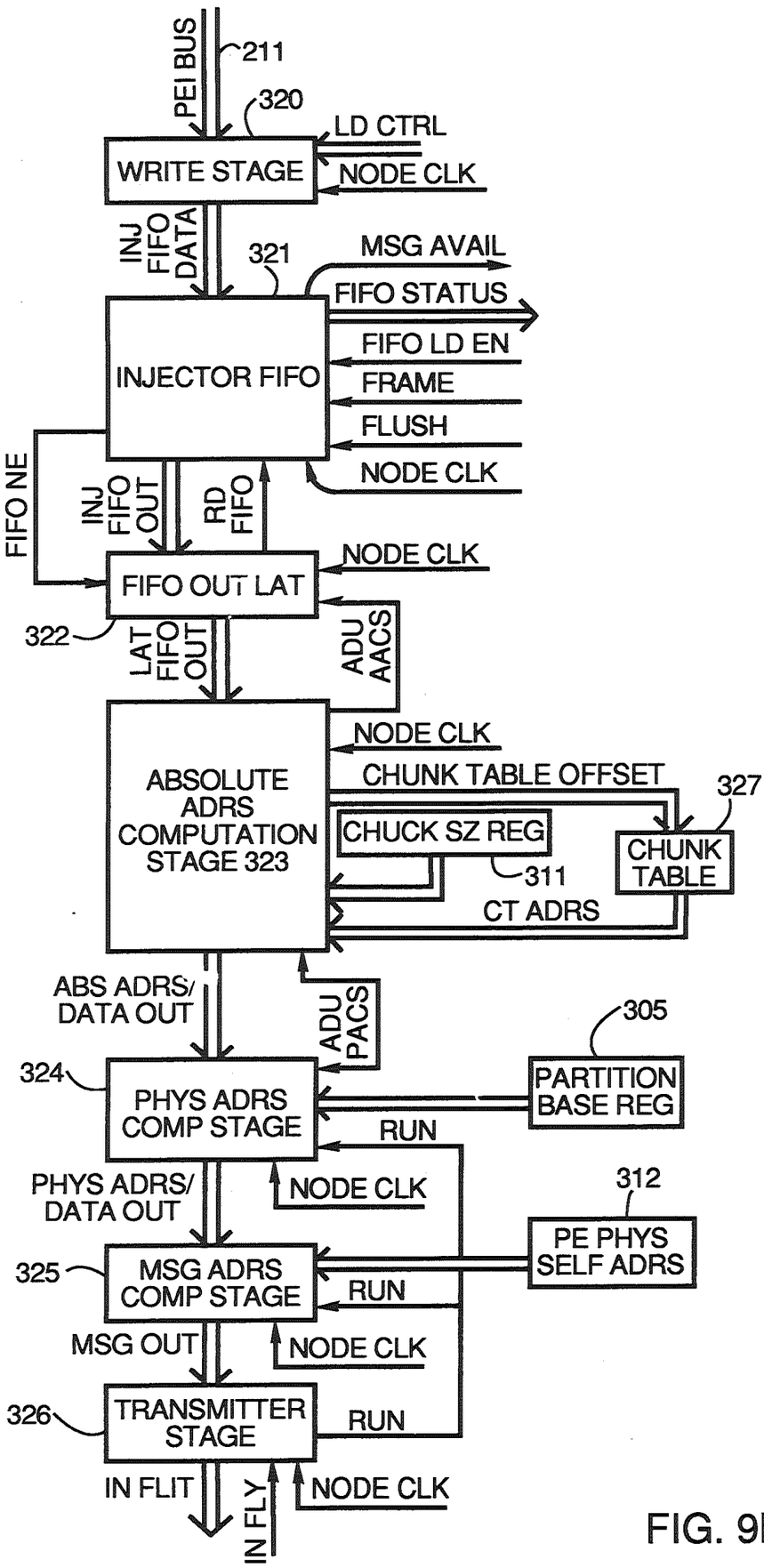
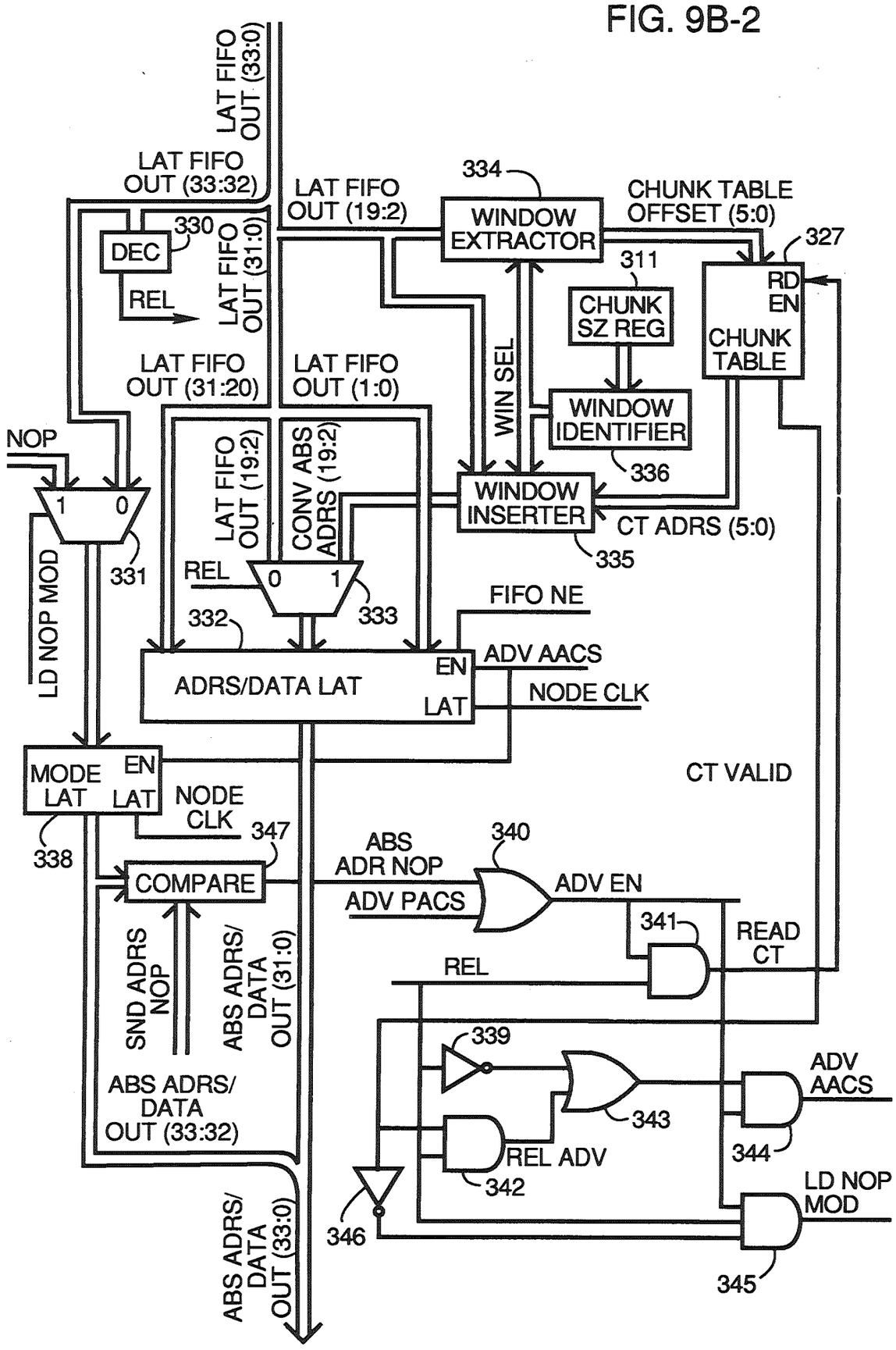

PEI BUS
211
320
LD CTRL
WRITE STAGE
NODE CLK
INJ FIFO DATA
321
MSG AVAIL
FIFO STATUS
INJECTOR FIFO
FIFO LD EN
FRAME
FLUSH
NODE CLK
FIFO NE
INJ FIFO OUT
RD FIFO
NODE CLK
FIFO OUT LAT
322
LAT FIFO OUT
ADU AACS
NODE CLK
ABSOLUTE ADRS COMPUTATION STAGE 323
CHUNK TABLE OFFSET
327
CHUCK SZ REG
CHUNK TABLE
311
CT ADRS
ABS ADRS/ DATA OUT
ADU PACS
305
324
PHYS ADRS COMP STAGE
PARTITION BASE REG
RUN
NODE CLK
PHYS ADRS/ DATA OUT
312
PE PHYS SELF ADRS
325
MSG ADRS COMP STAGE
RUN
MSG OUT
NODE CLK
326
TRANSMITTER STAGE
RUN
IN FLIT
IN FLY
NODE CLK

FIG. 9B-1

FIG. 9B-2


LAT FIFO OUT (33:0)
LAT FIFO OUT (33:32)
LAT FIFO OUT (19:2)
334
WINDOW EXTRACTOR
CHUNK TABLE OFFSET (5:0)
327
330
DEC
REL
LAT FIFO OUT (31:0)
311
CHUNK SZ REG
RD EN
CHUNK TABLE
LAT FIFO OUT (31:20)
LAT FIFO OUT (1:0)
WIN SEL
WINDOW IDENTIFIER
336
NOP
1
0
331
LAT FIFO OUT (19:2)
CONV ABS ADRS (19:2)
WINDOW INSERTER
CT ADRS (5:0)
335
REL
0
1
333
FIFO NE
332
ADV AACS
EN
ADRS/DATA LAT
LAT
NODE CLK
LD NOP MOD
CT VALID
MODE LAT
EN
LAT
NODE CLK
347
338
COMPARE
ABS ADR NOP
340
ADV PACS
ADV EN
341
READ CT
REL
SND ADRS NOP
ABS ADRS/ DATA OUT (31:0)
339
ADV AACS
343
344
ABS ADRS/ DATA OUT (33:32)
REL ADV
342
LD NOP MOD
346
345
ABS ADRS/ DATA OUT (33:0)

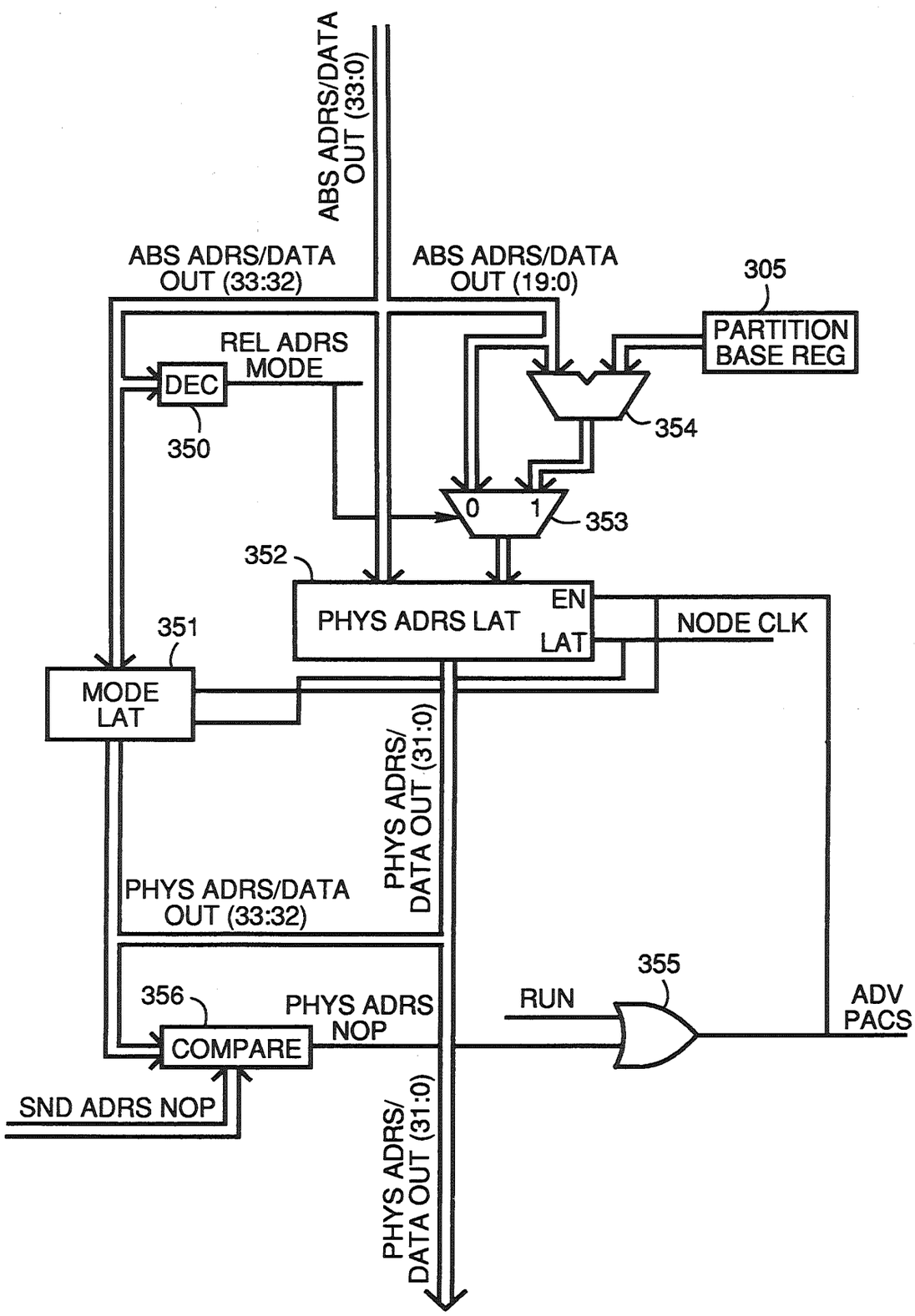

ABS ADRS/DATA OUT (33:0)
ABS ADRS/DATA OUT (33:32)
ABS ADRS/DATA OUT (19:0)
305
PARTITION BASE REG
REL ADRS MODE
DEC
350
354
0
1
353
352
PHYS ADRS LAT
EN
LAT
NODE CLK
351
MODE LAT
PHYS ADRS/ DATA OUT (31:0)
PHYS ADRS/DATA OUT (33:32)
355
356
PHYS ADRS NOP
RUN
ADV PACS
COMPARE
SND ADRS NOP
PHYS ADRS/ DATA OUT (31:0)

FIG. 9B-3

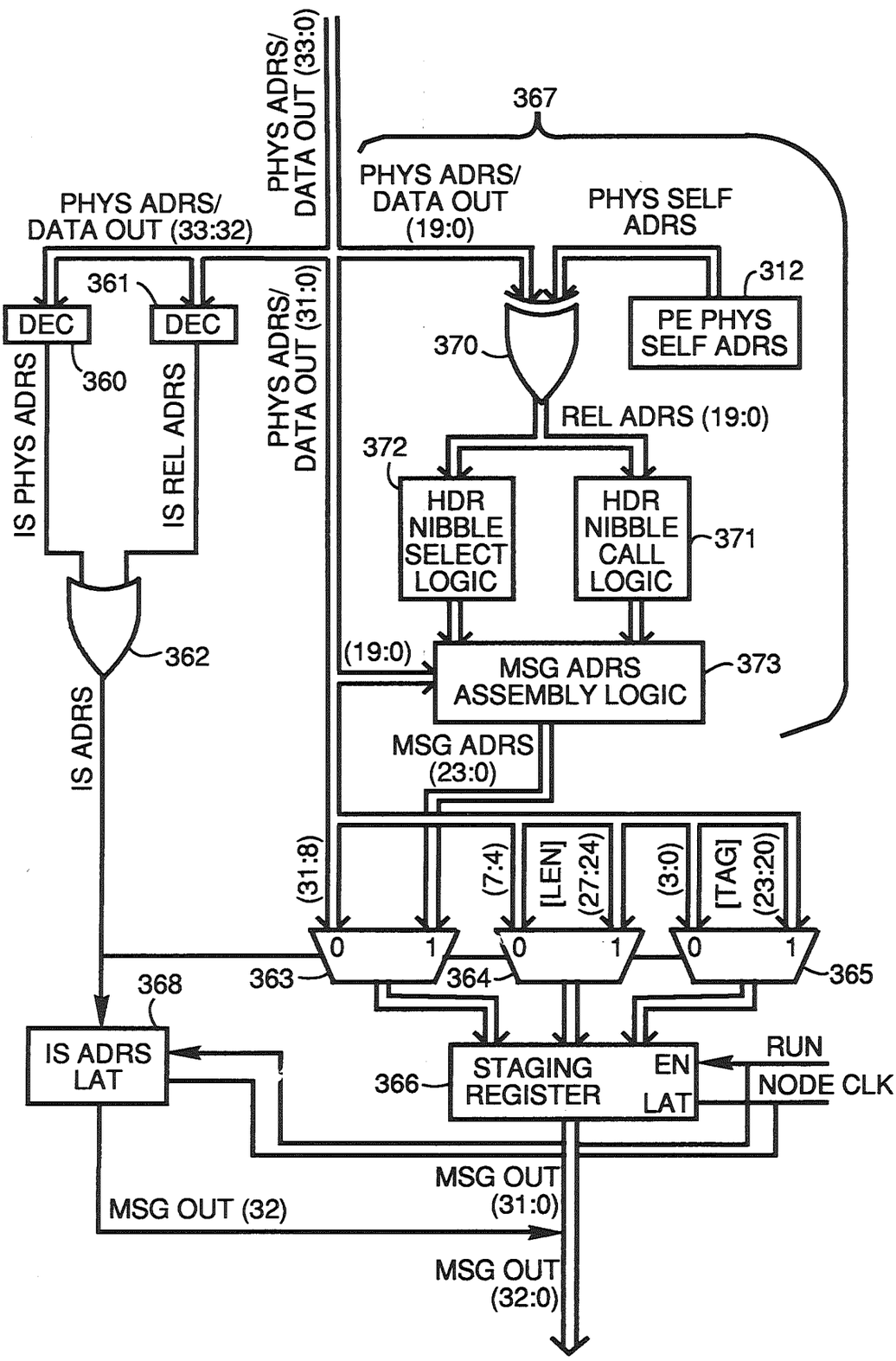

PHYS ADRS/
DATA OUT (33:0)
367
PHYS ADRS/
DATA OUT
(19:0)
PHYS SELF
ADRS
PHYS ADRS/
DATA OUT (33:32)
361
DEC
DEC
360
312
PE PHYS
SELF ADRS
370
REL ADRS (19:0)
372
HDR
NIBBLE
SELECT
LOGIC
HDR
NIBBLE
CALL
LOGIC
371
IS PHYS ADRS
IS REL ADRS
PHYS ADRS/
DATA OUT (31:0)
362
(19:0)
MSG ADRS
ASSEMBLY LOGIC
373
IS ADRS
MSG ADRS
(23:0)
(31:8)
(7:4)
[LEN]
(27:24)
(3:0)
[TAG]
(23:20)
0
1
363
364
365
368
IS ADRS
LAT
366
STAGING
REGISTER
EN
LAT
RUN
NODE CLK
MSG OUT
(31:0)
MSG OUT (32)
MSG OUT
(32:0)

FIG. 9B-4

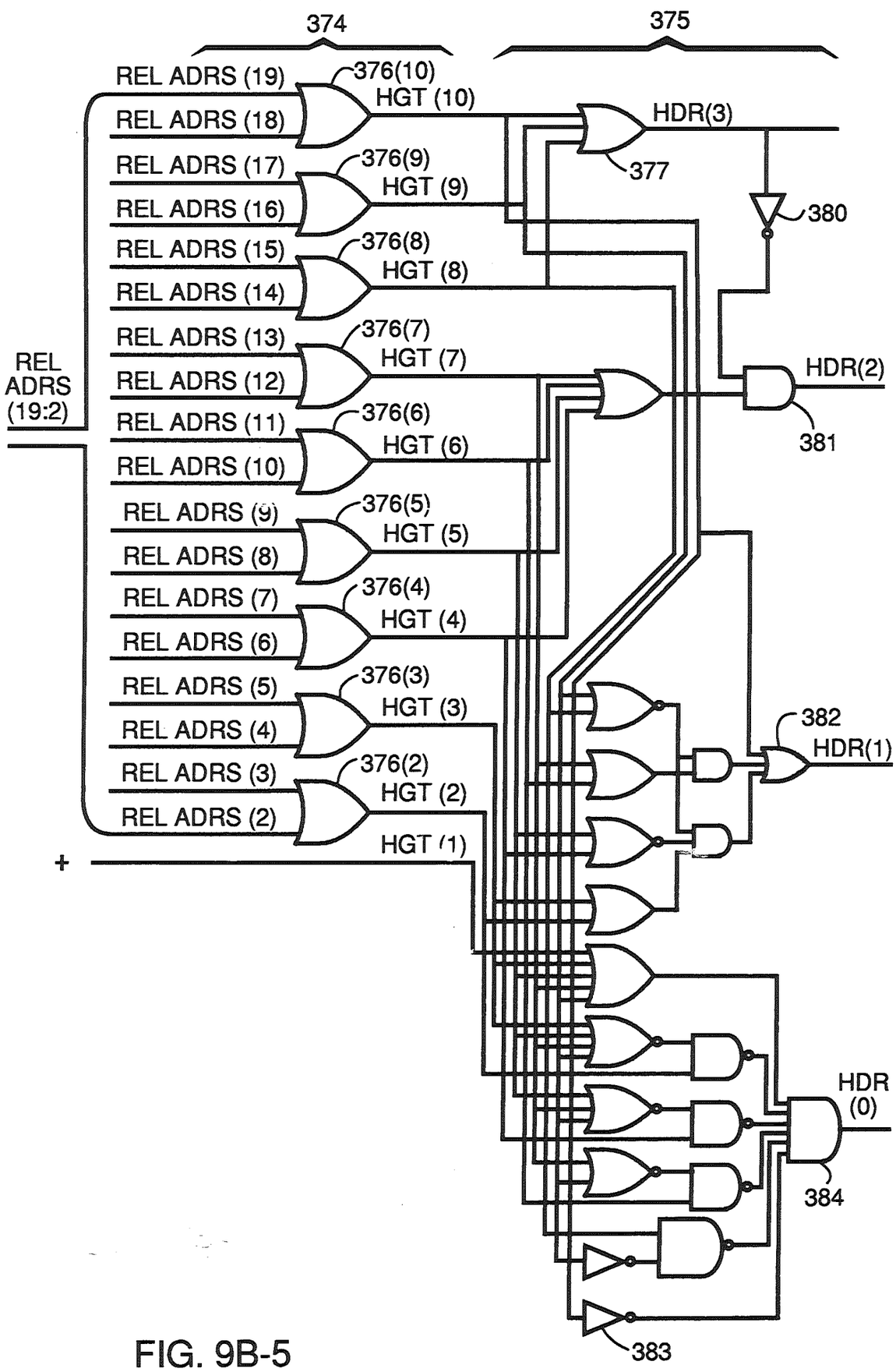

374
375
REL ADRS (19)
REL ADRS (18)
REL ADRS (17)
REL ADRS (16)
REL ADRS (15)
REL ADRS (14)
REL ADRS (13)
REL ADRS (12)
REL ADRS (11)
REL ADRS (10)
REL ADRS (9)
REL ADRS (8)
REL ADRS (7)
REL ADRS (6)
REL ADRS (5)
REL ADRS (4)
REL ADRS (3)
REL ADRS (2)
REL ADRS (19:2)
+
376(10)
HGT (10)
376(9)
HGT (9)
376(8)
HGT (8)
376(7)
HGT (7)
376(6)
HGT (6)
376(5)
HGT (5)
376(4)
HGT (4)
376(3)
HGT (3)
376(2)
HGT (2)
HGT (1)
HDR(3)
377
380
HDR(2)
381
382
HDR(1)
HDR
(0)
384
383

FIG. 9B-5

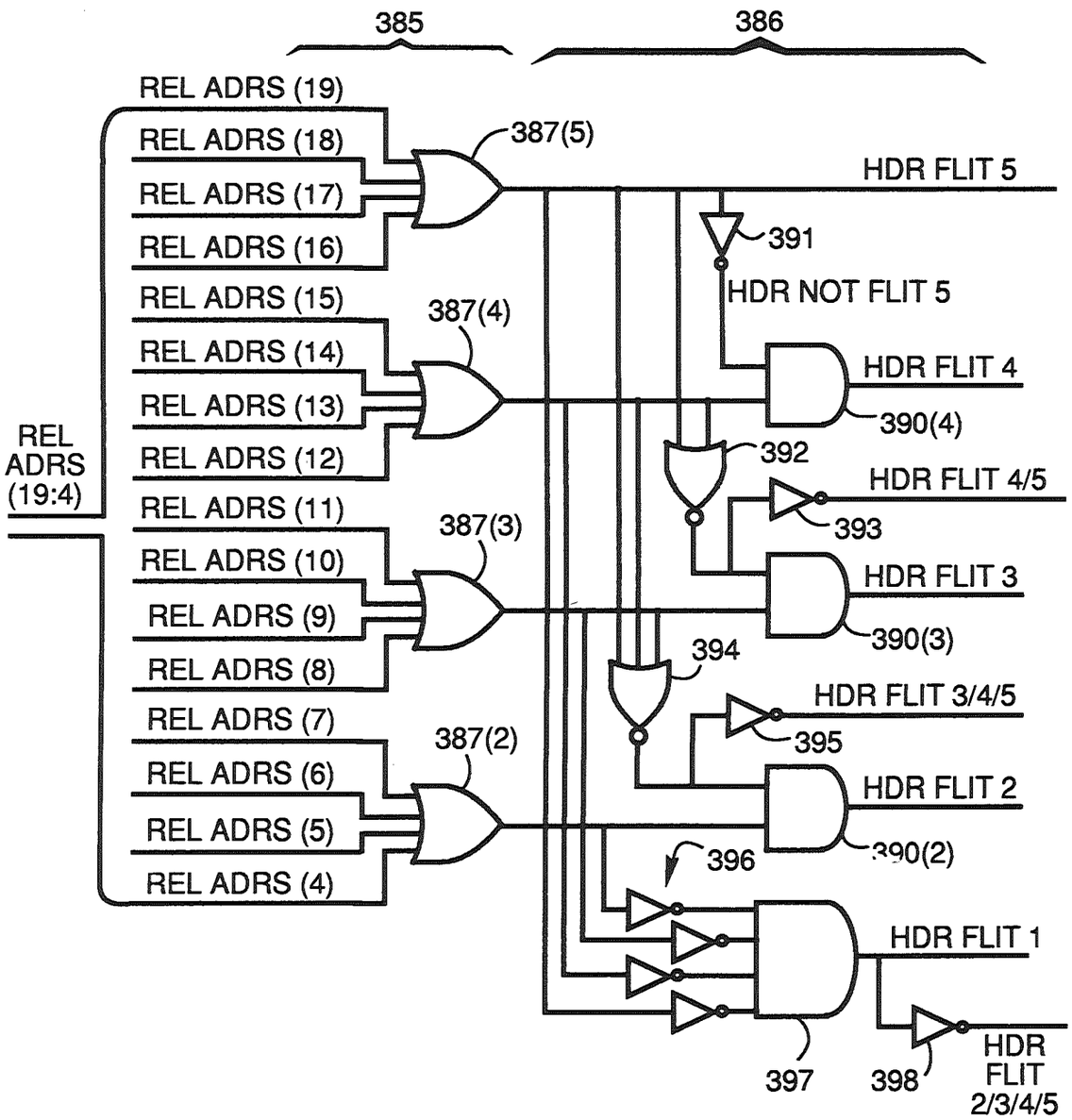

385
386
REL ADRS (19)
REL ADRS (18)
REL ADRS (17)
REL ADRS (16)
REL ADRS (15)
REL ADRS (14)
REL ADRS (13)
REL ADRS (12)
REL ADRS (11)
REL ADRS (10)
REL ADRS (9)
REL ADRS (8)
REL ADRS (7)
REL ADRS (6)
REL ADRS (5)
REL ADRS (4)
REL ADRS (19:4)
387(5)
387(4)
387(3)
387(2)
HDR FLIT 5
391
HDR NOT FLIT 5
HDR FLIT 4
390(4)
392
HDR FLIT 4/5
393
HDR FLIT 3
390(3)
394
HDR FLIT 3/4/5
395
HDR FLIT 2
390(2)
396
HDR FLIT 1
397
398
HDR FLIT 2/3/4/5

FIG. 9B-6

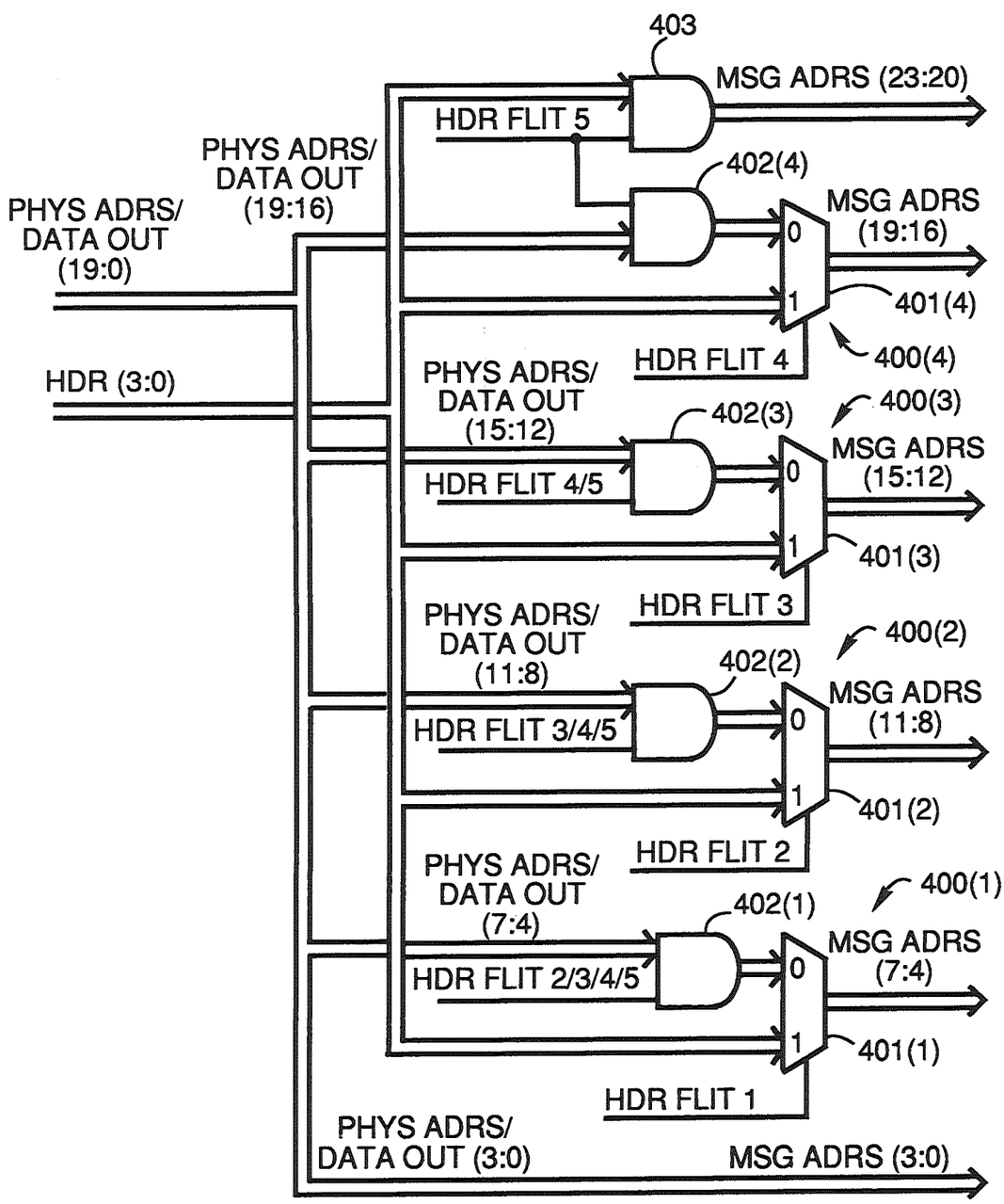

403
MSG ADRS (23:20)
HDR FLIT 5
PHYS ADRS/
DATA OUT
(19:16)
402(4)
PHYS ADRS/
DATA OUT
(19:0)
MSG ADRS
(19:16)
0
1
401(4)
400(4)
HDR FLIT 4
HDR (3:0)
PHYS ADRS/
DATA OUT
(15:12)
402(3)
400(3)
MSG ADRS
(15:12)
HDR FLIT 4/5
401(3)
HDR FLIT 3
PHYS ADRS/
DATA OUT
(11:8)
400(2)
402(2)
MSG ADRS
(11:8)
HDR FLIT 3/4/5
401(2)
HDR FLIT 2
PHYS ADRS/
DATA OUT
(7:4)
400(1)
402(1)
MSG ADRS
(7:4)
HDR FLIT 2/3/4/5
401(1)
HDR FLIT 1
PHYS ADRS/
DATA OUT (3:0)
MSG ADRS (3:0)

FIG. 9B-7

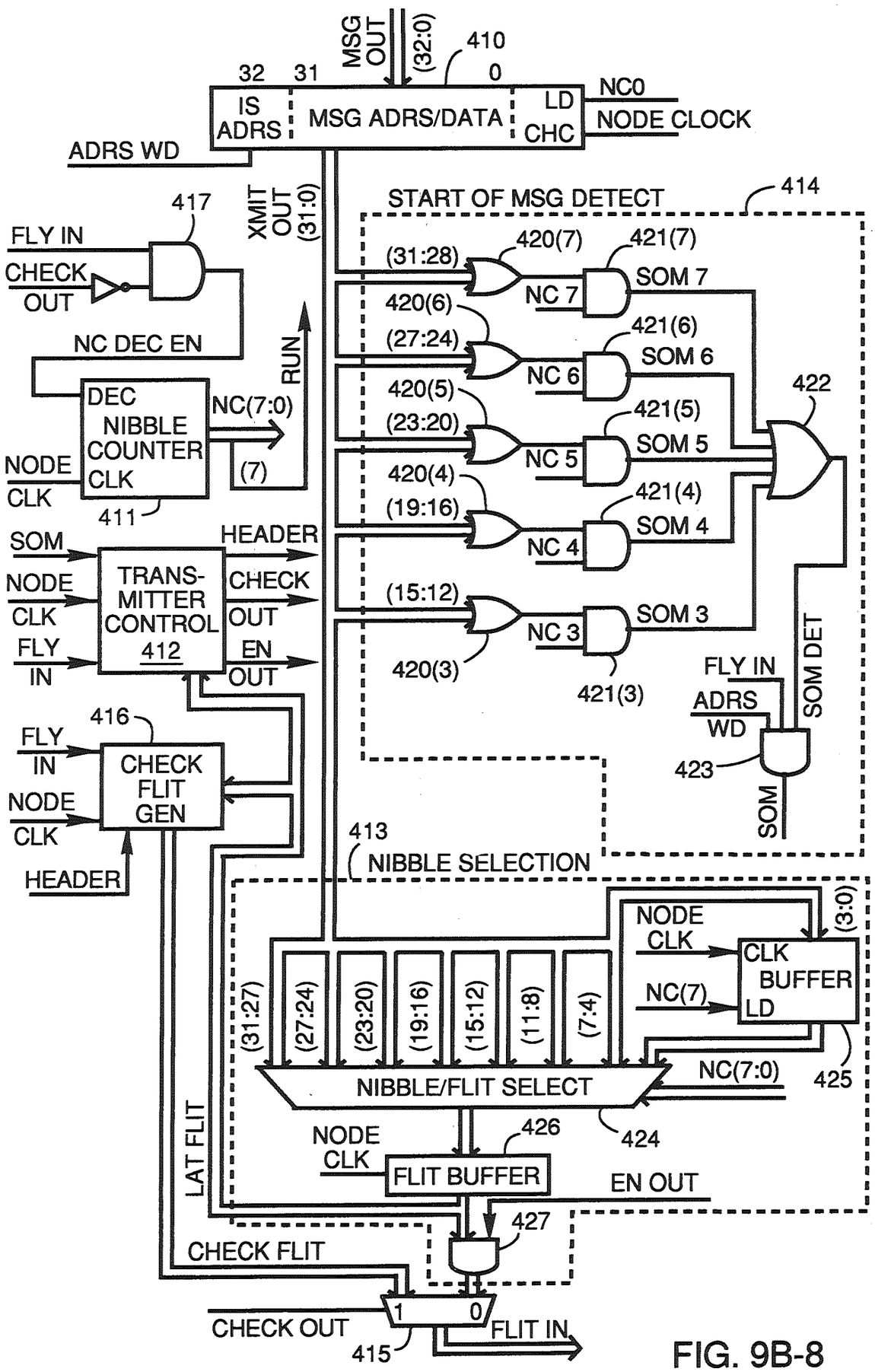

MSG OUT
(32:0)
410
32
31
0
IS ADRS
MSG ADRS/DATA
LD CHC
NC0
NODE CLOCK
ADRS WD
XMIT OUT (31:0)
START OF MSG DETECT
414
417
FLY IN
CHECK OUT
NC DEC EN
DEC NIBBLE COUNTER
NC(7:0)
(7)
RUN
NODE CLK
411
(31:28)
420(7)
421(7)
NC 7
SOM 7
420(6)
(27:24)
421(6)
NC 6
SOM 6
422
420(5)
(23:20)
421(5)
NC 5
SOM 5
420(4)
(19:16)
421(4)
NC 4
SOM 4
(15:12)
NC 3
SOM 3
420(3)
421(3)
SOM
HEADER
TRANS-MITTER CONTROL 412
CHECK OUT
EN OUT
FLY IN
ADRS WD
SOM DET
423
416
CHECK FLIT GEN
413
NIBBLE SELECTION
NODE CLK
(3:0)
CLK BUFFER
NC(7)
LD
(31:27)
(27:24)
(23:20)
(19:16)
(15:12)
(11:8)
(7:4)
NC(7:0)
425
NIBBLE/FLIT SELECT
424
426
FLIT BUFFER
EN OUT
LAT FLIT
427
CHECK FLIT
1
0
CHECK OUT
FLIT IN
415

FIG. 9B-8

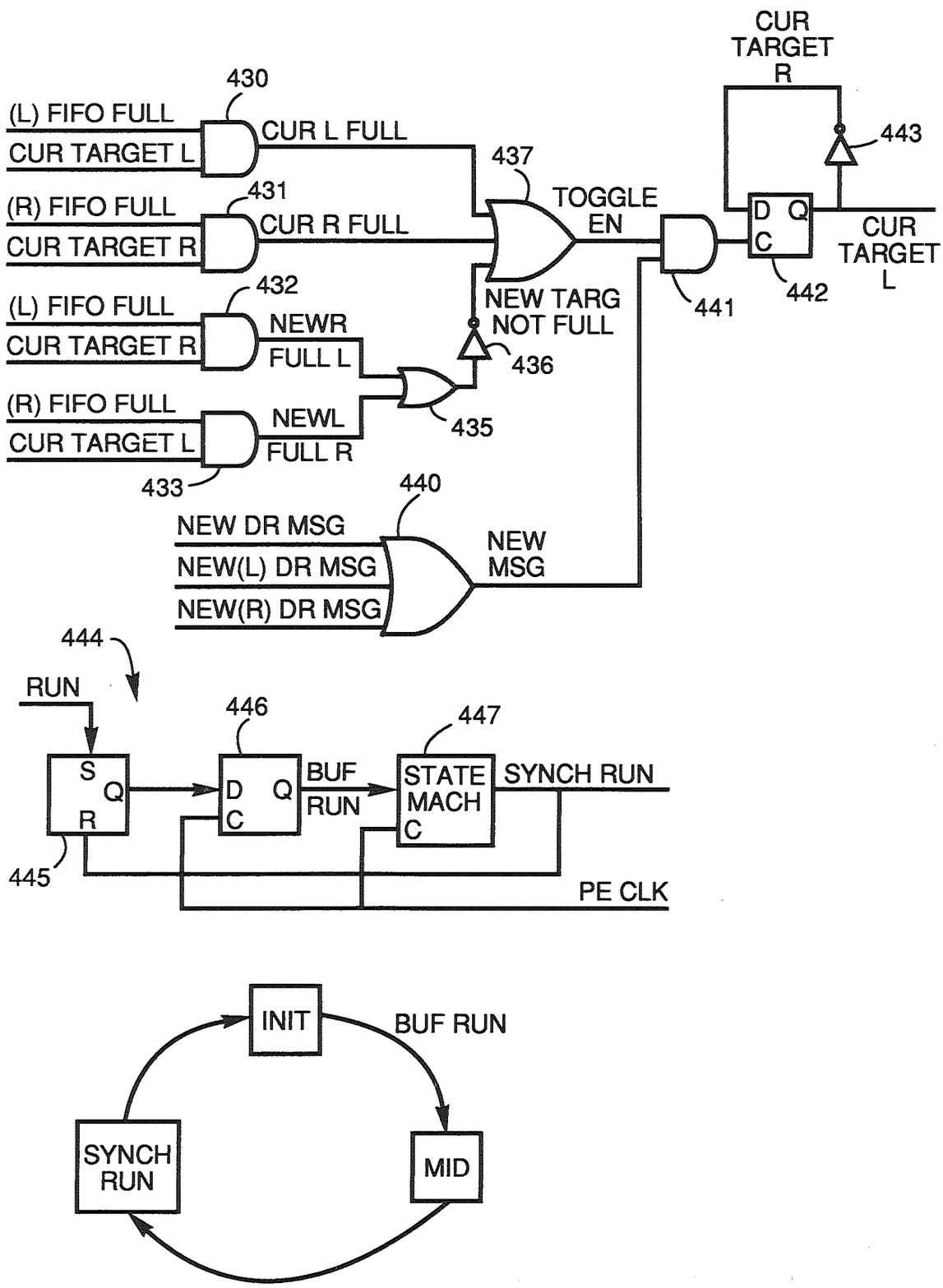

CUR TARGET R
430
(L) FIFO FULL
CUR TARGET L
CUR L FULL
437
443
(R) FIFO FULL
CUR TARGET R
431
CUR R FULL
TOGGLE EN
D Q
C
CUR TARGET L
442
NEW TARG NOT FULL
441
432
(L) FIFO FULL
CUR TARGET R
NEWR FULL L
436
(R) FIFO FULL
CUR TARGET L
NEWL FULL R
435
433
440
NEW DR MSG
NEW(L) DR MSG
NEW(R) DR MSG
NEW MSG
444
RUN
446
447
S
R
Q
D
C
BUF RUN
STATE MACH
C
SYNCH RUN
445
PE CLK
INIT
BUF RUN
SYNCH RUN
MID

FIG. 9B-9

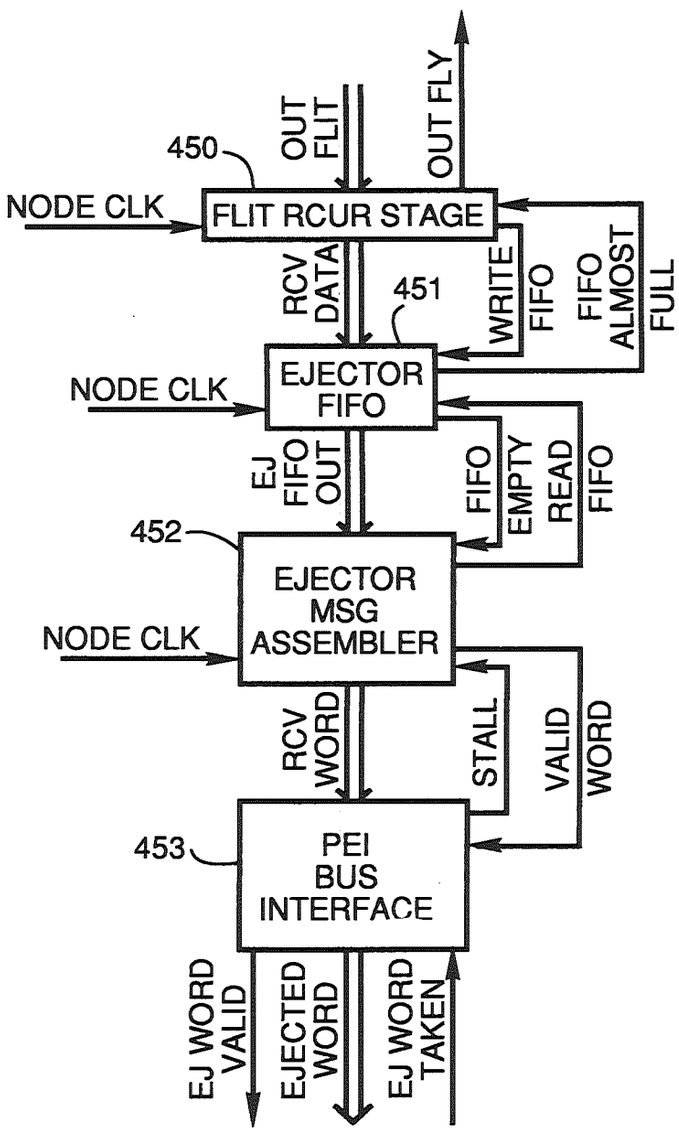

450
OUT FLIT
OUT FLY
NODE CLK
FLIT RCUR STAGE
RCV DATA
451
WRITE FIFO
FIFO ALMOST FULL
NODE CLK
EJECTOR FIFO
EJ FIFO OUT
FIFO EMPTY
READ FIFO
452
EJECTOR MSG ASSEMBLER
NODE CLK
RCV WORD
STALL
VALID WORD
453
PEI BUS INTERFACE
EJ WORD VALID
EJECTED WORD
EJ WORD TAKEN

FIG. 9C-1

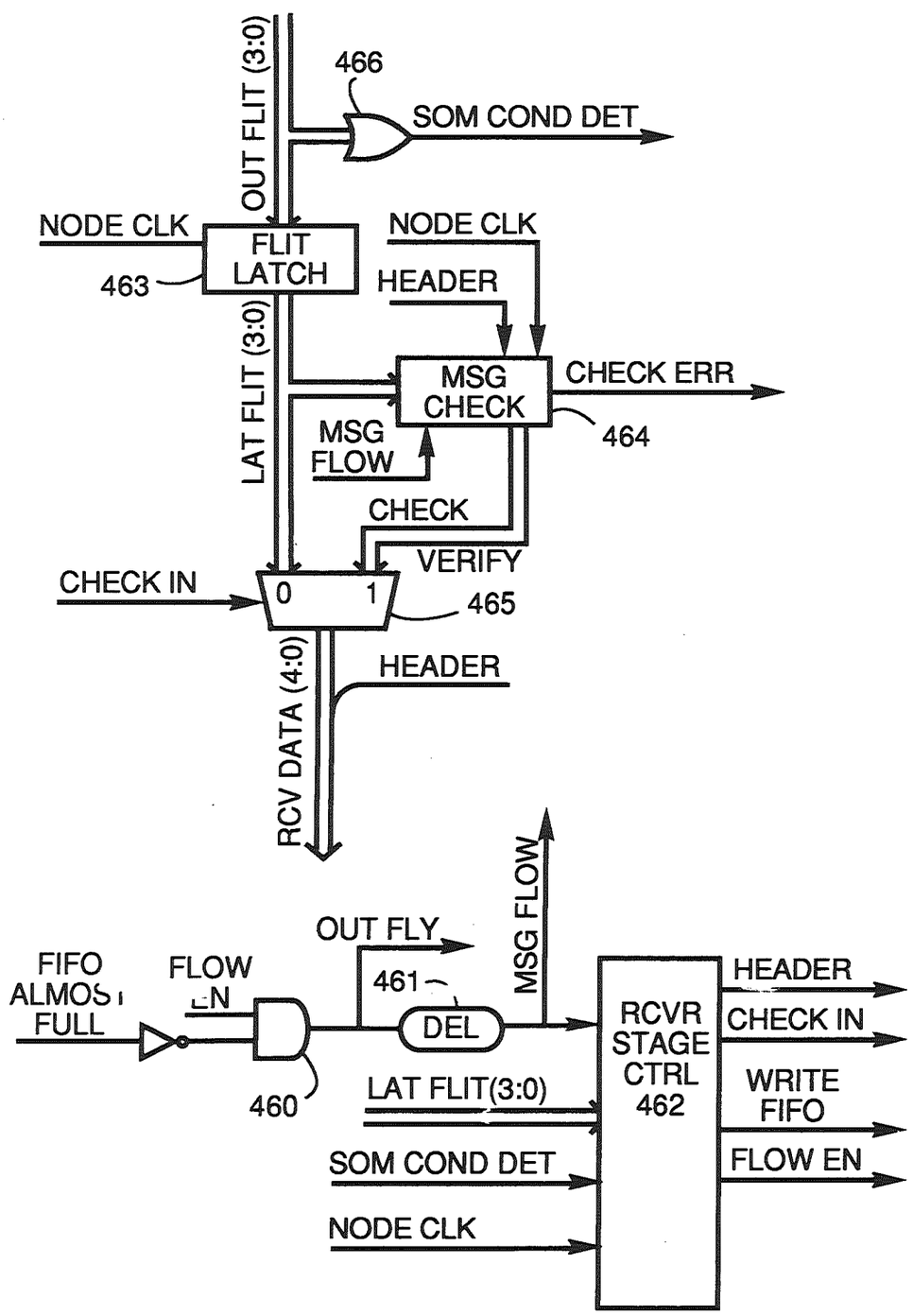
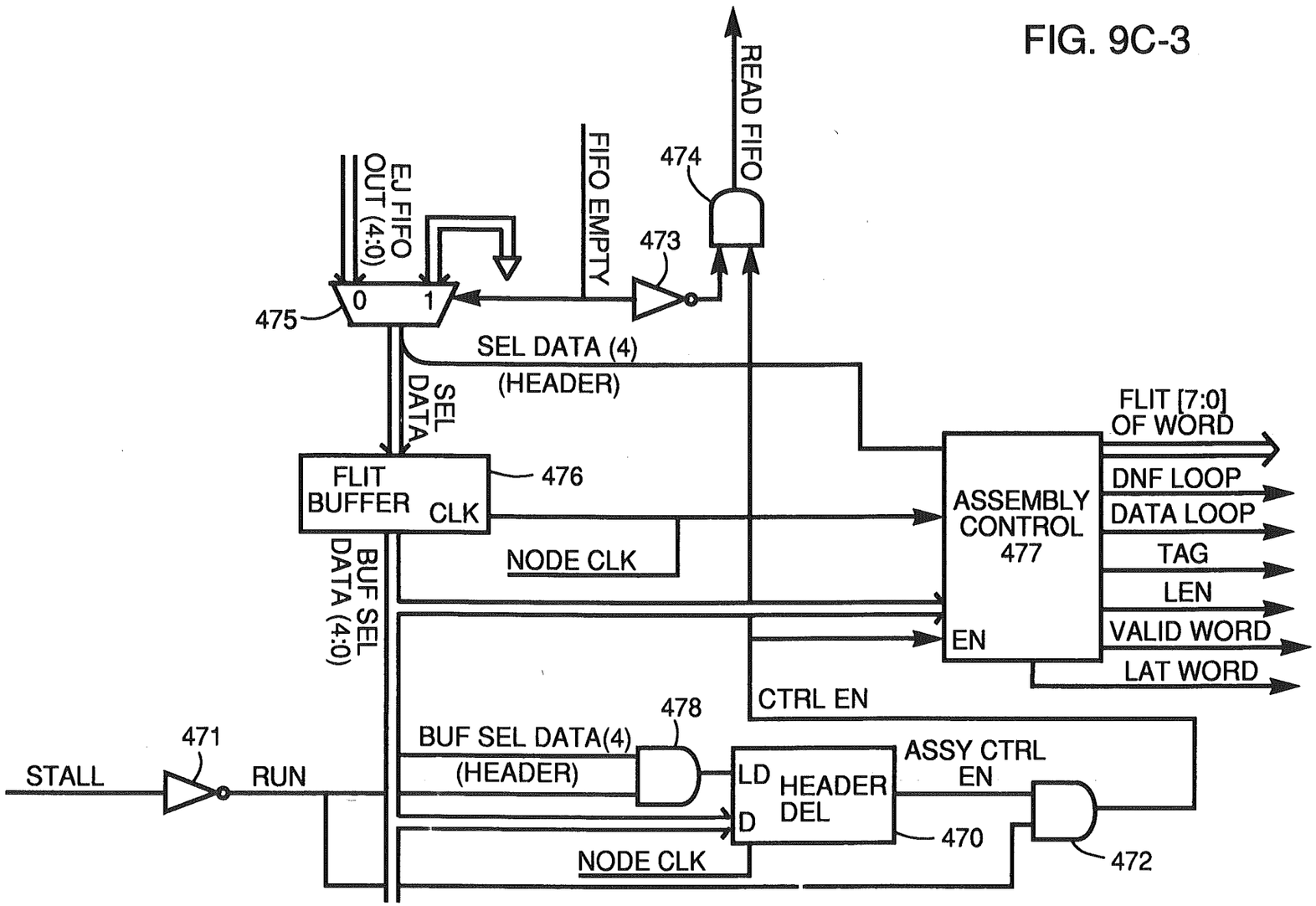

OUT FLIT (3:0)
466
SOM COND DET
NODE CLK
FLIT LATCH
463
NODE CLK
HEADER
LAT FLIT (3:0)
MSG CHECK
CHECK ERR
464
MSG FLOW
CHECK
VERIFY
CHECK IN
0
1
465
RCV DATA (4:0)
HEADER
MSG FLOW
OUT FLY
461
FIFO ALMOST FULL
FLOW EN
DEL
460
LAT FLIT(3:0)
SOM COND DET
NODE CLK
RCVR STAGE CTRL 462
HEADER
CHECK IN
WRITE FIFO
FLOW EN

FIG. 9C-2

FIG. 9C-3


READ FIFO
474
FIFO EMPTY
473
EJ FIFO OUT (4:0)
0
1
475
SEL DATA (4)
(HEADER)
SEL DATA
FLIT BUFFER
CLK
476
NODE CLK
BUF SEL DATA (4:0)
ASSEMBLY CONTROL 477
EN
FLIT [7:0] OF WORD
DNF LOOP
DATA LOOP
TAG
LEN
VALID WORD
LAT WORD
CTRL EN
478
BUF SEL DATA(4)
(HEADER)
LD
D
HEADER DEL
470
ASSY CTRL EN
472
471
STALL
RUN
NODE CLK

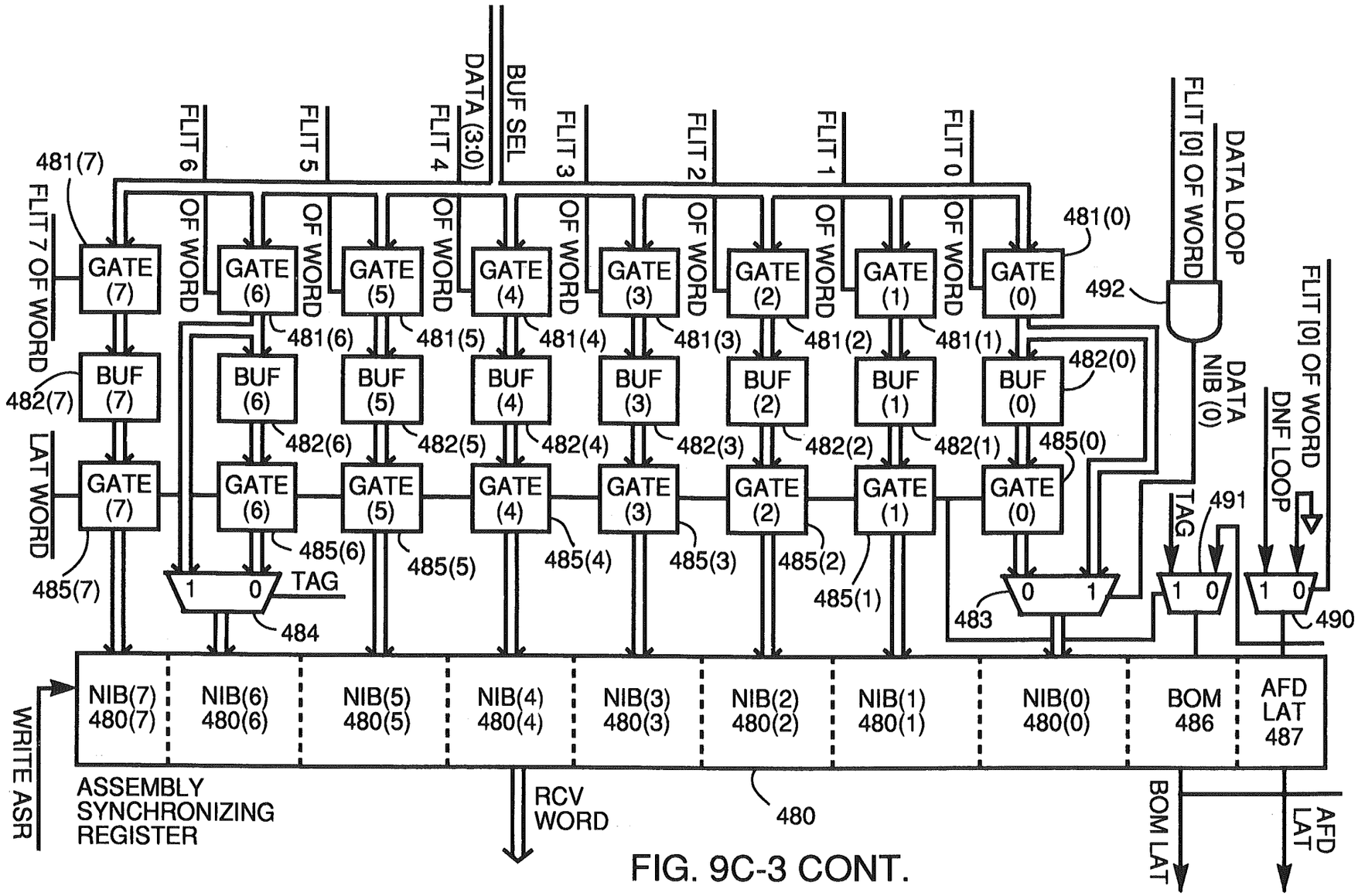

FLIT 6
FLIT 5
FLIT 4
DATA (3:0)
BUF SEL
FLIT 3
FLIT 2
FLIT 1
FLIT 0
FLIT [0] OF WORD
DATA LOOP
481(7)
FLIT 7 OF WORD
OF WORD
481(0)
492
GATE (7)
GATE (6)
GATE (5)
GATE (4)
GATE (3)
GATE (2)
GATE (1)
GATE (0)
481(6)
481(5)
481(4)
481(3)
481(2)
481(1)
BUF (7)
BUF (6)
BUF (5)
BUF (4)
BUF (3)
BUF (2)
BUF (1)
BUF (0)
482(0)
482(7)
482(6)
482(5)
482(4)
482(3)
482(2)
482(1)
485(0)
DATA NIB (0)
DNF LOOP
FLIT [0] OF WORD
LAT WORD
TAG
491
485(7)
485(6)
485(5)
485(4)
485(3)
485(2)
485(1)
1 0
TAG
484
0 1
483
1 0
1 0
490
NIB(7) 480(7)
NIB(6) 480(6)
NIB(5) 480(5)
NIB(4) 480(4)
NIB(3) 480(3)
NIB(2) 480(2)
NIB(1) 480(1)
NIB(0) 480(0)
BOM 486
AFD LAT 487
WRITE ASR
ASSEMBLY SYNCHRONIZING REGISTER
RCV WORD
480
BOM LAT
AFD LAT

FIG. 9C-3 CONT.

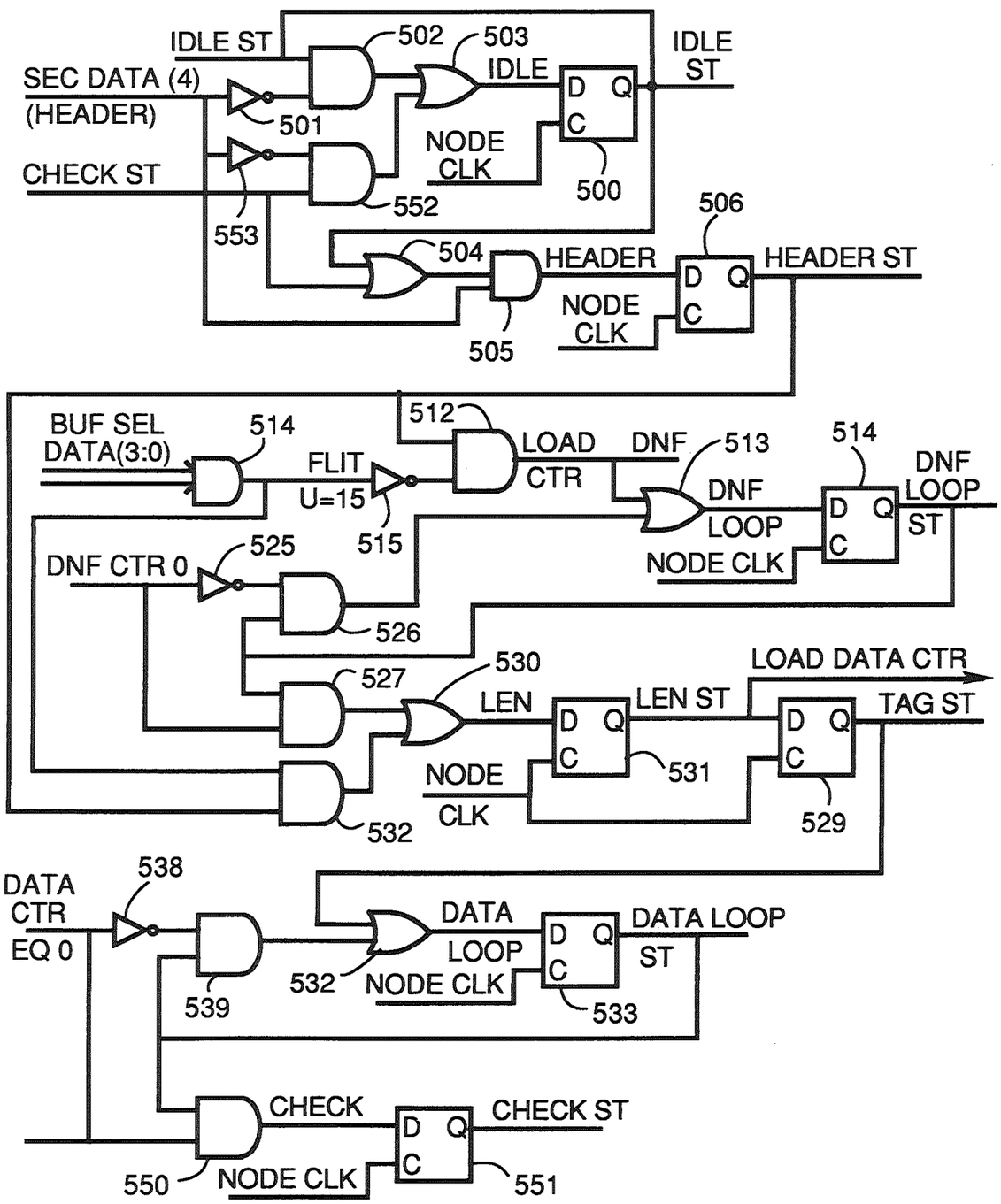

IDLE ST
502
503
IDLE
IDLE ST
SEC DATA (4)
(HEADER)
501
D Q
C
NODE CLK
500
CHECK ST
552
553
506
504
HEADER
HEADER ST
D Q
C
NODE CLK
505
BUF SEL DATA(3:0)
514
512
LOAD CTR
DNF
513
514
DNF LOOP ST
FLIT U=15
515
DNF
LOOP
NODE CLK
DNF CTR 0
525
526
527
530
LOAD DATA CTR
LEN
LEN ST
TAG ST
531
NODE CLK
529
532
538
DATA CTR EQ 0
DATA LOOP ST
DATA LOOP
539
532
NODE CLK
533
CHECK
CHECK ST
550
NODE CLK
551

FIG. 9C-4

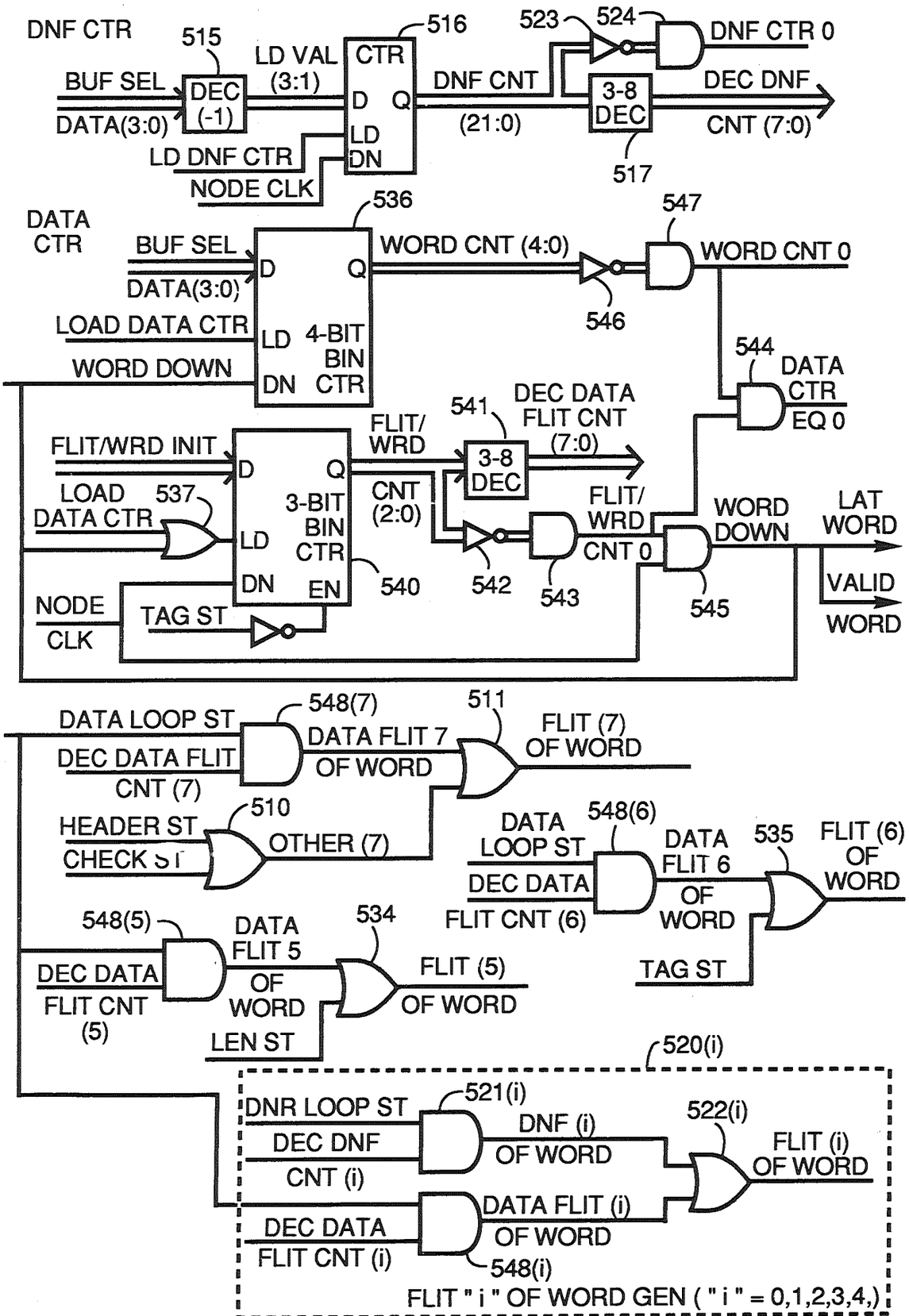

DNF CTR
515
LD VAL
(3:1)
516
CTR
523
524
DNF CTR 0
BUF SEL
DEC
(-1)
DATA(3:0)
D
Q
DNF CNT
(21:0)
3-8
DEC
DEC DNF
CNT (7:0)
LD
DN
LD DNF CTR
NODE CLK
517
DATA
CTR
536
547
BUF SEL
DATA(3:0)
D
Q
WORD CNT (4:0)
WORD CNT 0
546
LOAD DATA CTR
LD
4-BIT
BIN
CTR
WORD DOWN
DN
544
DATA
CTR
EQ 0
541
DEC DATA
FLIT CNT
(7:0)
FLIT/
WRD
FLIT/WRD INIT
D
Q
3-8
DEC
LOAD
DATA CTR
537
3-BIT
BIN
CTR
CNT
(2:0)
FLIT/
WRD
CNT 0
WORD
DOWN
LAT
WORD
LD
DN
EN
540
542
543
545
VALID
WORD
NODE
CLK
TAG ST
548(7)
511
DATA LOOP ST
DEC DATA FLIT
CNT (7)
DATA FLIT 7
OF WORD
FLIT (7)
OF WORD
510
HEADER ST
CHECK ST
OTHER (7)
548(6)
DATA
LOOP ST
DEC DATA
FLIT CNT (6)
DATA
FLIT 6
OF
WORD
535
FLIT (6)
OF
WORD
TAG ST
548(5)
534
DATA
FLIT 5
OF
WORD
DEC DATA
FLIT CNT
(5)
FLIT (5)
OF WORD
LEN ST
520(i)
521(i)
DNR LOOP ST
DEC DNF
CNT (i)
DNF (i)
OF WORD
522(i)
FLIT (i)
OF WORD
DATA FLIT (i)
OF WORD
DEC DATA
FLIT CNT (i)
548(i)
FLIT " i " OF WORD GEN (" i " = 0,1,2,3,4,)

FIG. 9C-5

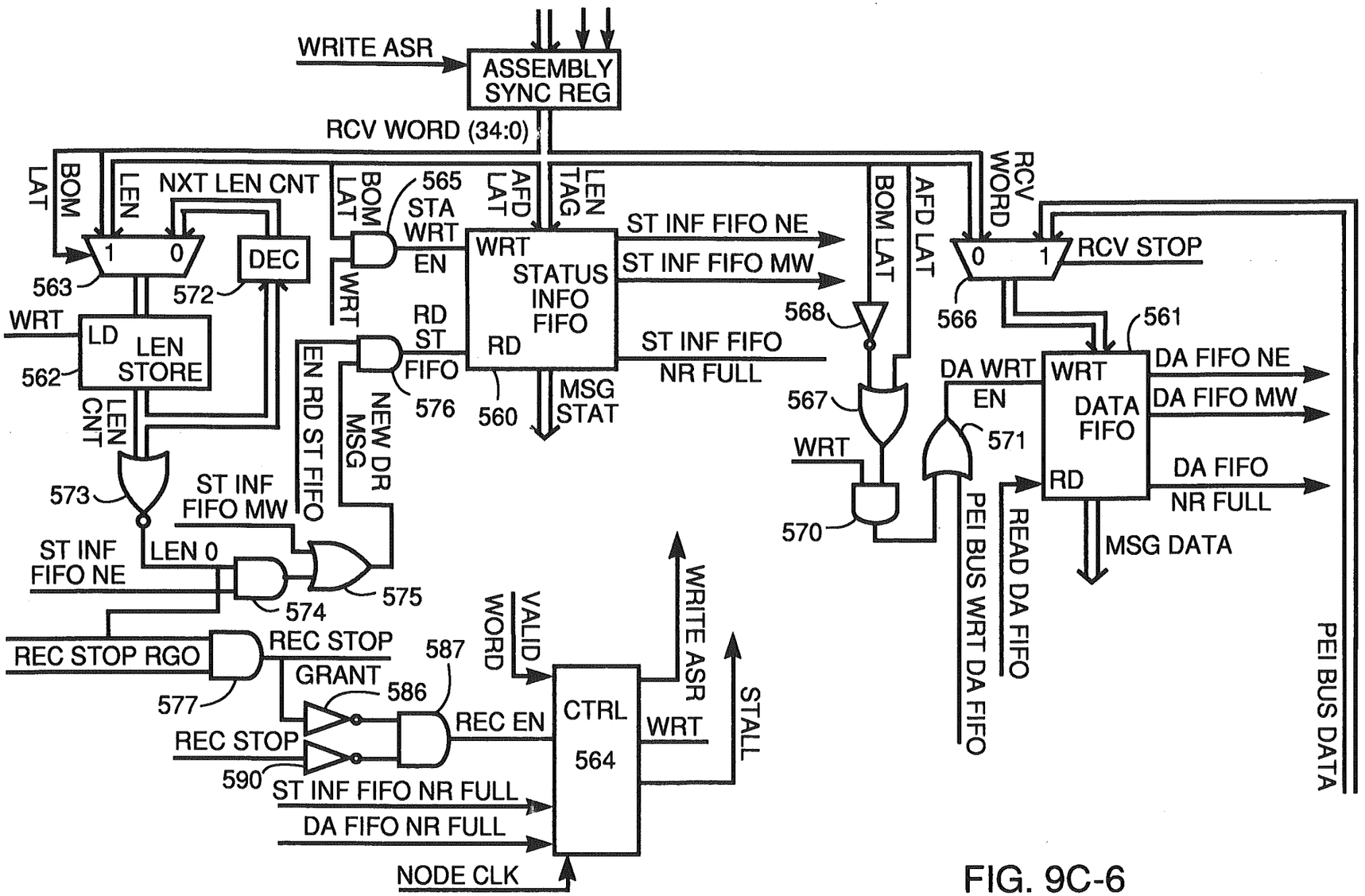

WRITE ASR
ASSEMBLY SYNC REG
RCV WORD (34:0)
BOM LAT
LEN
NXT LEN CNT
1
0
563
DEC
572
WRT
LD
LEN STORE
562
LEN CNT
573
ST INF FIFO MW
ST INF FIFO NE
LEN 0
574
575
REC STOP RGO
REC STOP GRANT
577
586
587
REC STOP
590
REC EN
ST INF FIFO NR FULL
DA FIFO NR FULL
NODE CLK
VALID WORD
CTRL
564
WRITE ASR
WRT
STALL
BOM LAT
565
STA WRT EN
AFD LAT
LEN TAG
WRT
RD ST FIFO
576
EN RD ST FIFO
NEW DR MSG
WRT
STATUS INFO FIFO
RD
560
MSG STAT
ST INF FIFO NE
ST INF FIFO MW
ST INF FIFO NR FULL
BOM LAT
AFD LAT
568
567
WRT
570
RCV WORD
0
1
RCV STOP
566
561
DA WRT EN
571
WRT
DATA FIFO
RD
DA FIFO NE
DA FIFO MW
DA FIFO NR FULL
MSG DATA
PEI BUS WRT DA FIFO
READ DA FIFO
PEI BUS DATA

FIG. 9C-6

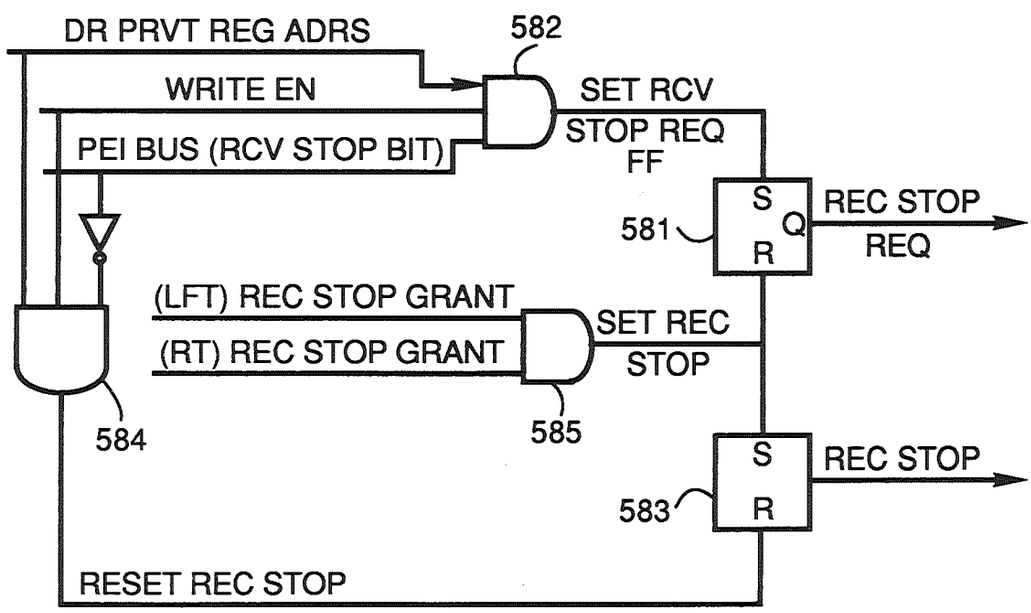
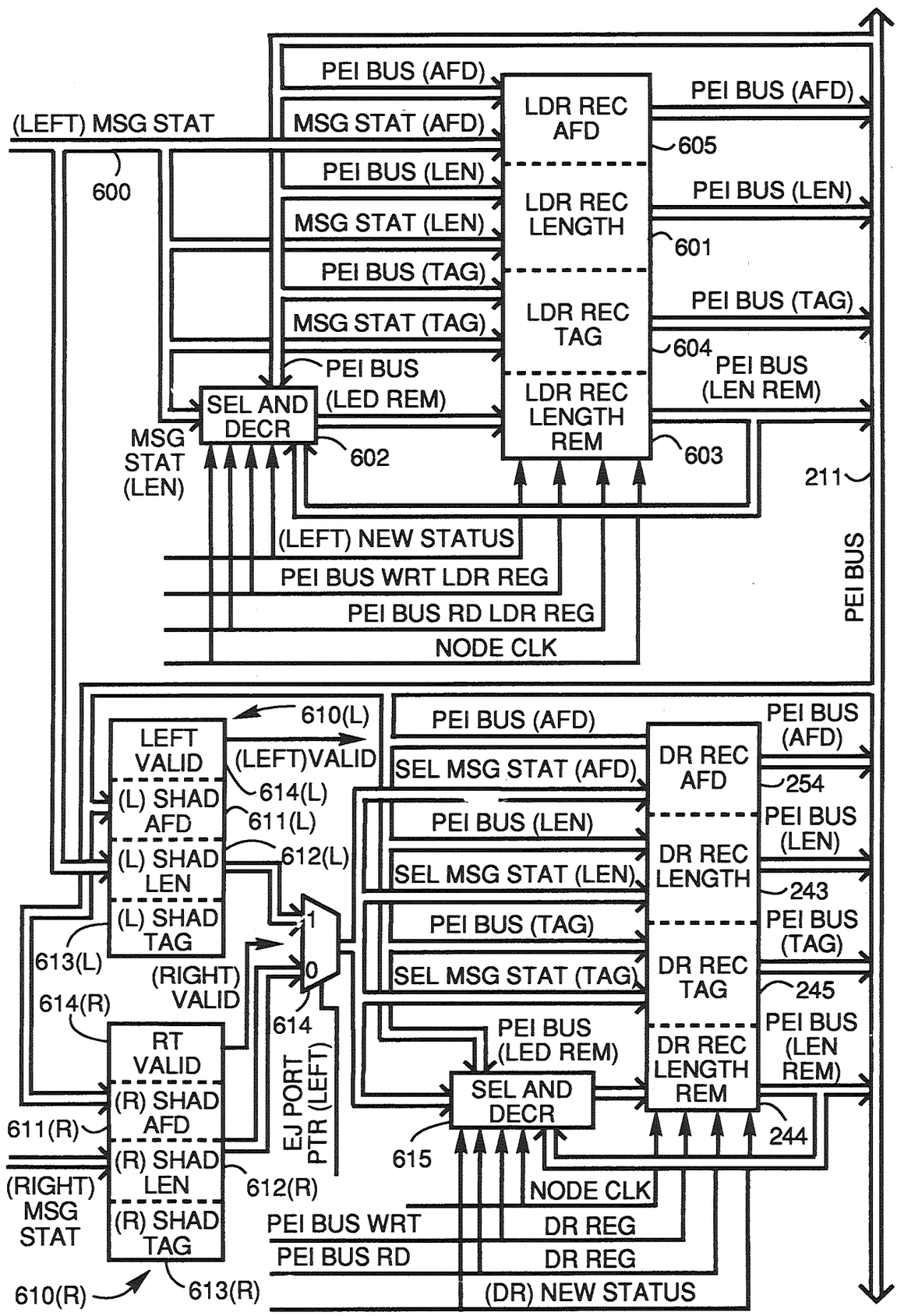

DR PRVT REG ADRS
582
WRITE EN
SET RCV
STOP REQ
FF
PEI BUS (RCV STOP BIT)
S
Q
REC STOP
REQ
581
R
(LFT) REC STOP GRANT
SET REC
STOP
(RT) REC STOP GRANT
584
585
S
REC STOP
583
R
RESET REC STOP

FIG. 9C-7

FIG. 9D-1


PEI BUS (AFD)
(LEFT) MSG STAT
MSG STAT (AFD)
LDR REC AFD
PEI BUS (AFD)
605
600
PEI BUS (LEN)
MSG STAT (LEN)
LDR REC LENGTH
PEI BUS (LEN)
601
PEI BUS (TAG)
MSG STAT (TAG)
LDR REC TAG
PEI BUS (TAG)
604
PEI BUS (LED REM)
SEL AND DECR
LDR REC LENGTH REM
PEI BUS (LEN REM)
MSG STAT (LEN)
602
603
211
(LEFT) NEW STATUS
PEI BUS WRT LDR REG
PEI BUS RD LDR REG
NODE CLK
PEI BUS
610(L)
LEFT VALID
(LEFT)VALID
614(L)
(L) SHAD AFD
611(L)
(L) SHAD LEN
612(L)
(L) SHAD TAG
613(L)
1
0
(RIGHT) VALID
614(R)
614
RT VALID
EJ PORT PTR (LEFT)
(R) SHAD AFD
611(R)
(R) SHAD LEN
612(R)
(RIGHT) MSG STAT
(R) SHAD TAG
610(R)
613(R)
PEI BUS (AFD)
SEL MSG STAT (AFD)
DR REC AFD
254
PEI BUS (AFD)
PEI BUS (LEN)
SEL MSG STAT (LEN)
DR REC LENGTH
243
PEI BUS (LEN)
PEI BUS (TAG)
SEL MSG STAT (TAG)
DR REC TAG
245
PEI BUS (TAG)
PEI BUS (LED REM)
SEL AND DECR
DR REC LENGTH REM
PEI BUS (LEN REM)
615
244
NODE CLK
PEI BUS WRT
DR REG
PEI BUS RD
DR REG
(DR) NEW STATUS

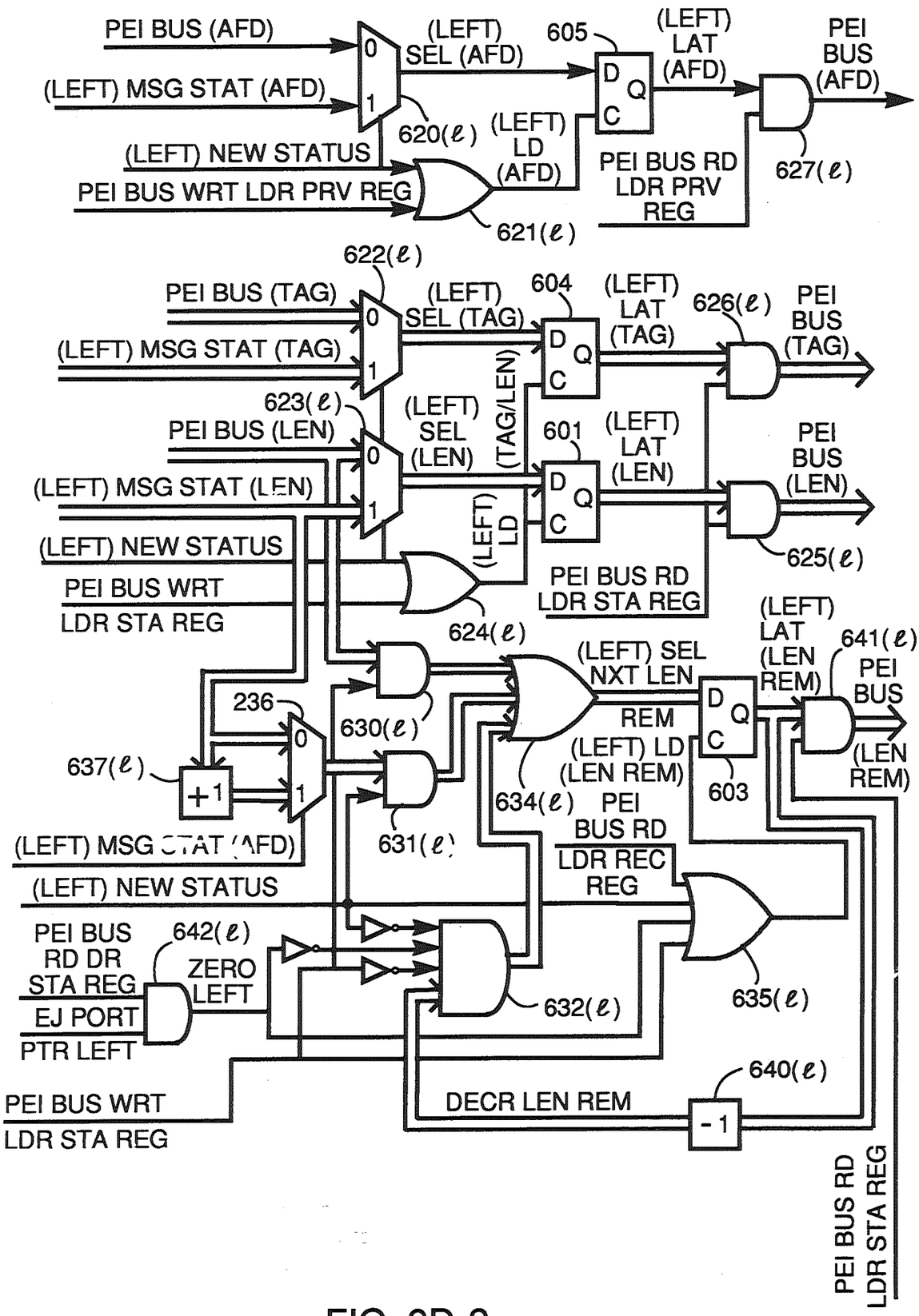

PEI BUS (AFD)
(LEFT) MSG STAT (AFD)
(LEFT) NEW STATUS
PEI BUS WRT LDR PRV REG
(LEFT) SEL (AFD)
620(e)
(LEFT) LD (AFD)
621(e)
605
(LEFT) LAT (AFD)
PEI BUS RD LDR PRV REG
PEI BUS (AFD)
627(e)
622(e)
PEI BUS (TAG)
(LEFT) MSG STAT (TAG)
(LEFT) SEL (TAG)
604
(LEFT) LAT (TAG)
626(e)
PEI BUS (TAG)
623(e)
PEI BUS (LEN)
(LEFT) MSG STAT (LEN)
(LEFT) SEL (LEN)
(TAG/LEN)
601
(LEFT) LAT (LEN)
PEI BUS (LEN)
625(e)
(LEFT) NEW STATUS
PEI BUS WRT LDR STA REG
(LEFT) LD
PEI BUS RD LDR STA REG
624(e)
(LEFT) LAT (LEN REM)
641(e)
PEI BUS
(LEN REM)
(LEFT) SEL NXT LEN REM
(LEFT) LD (LEN REM)
603
236
630(e)
637(e)
+1
634(e)
PEI BUS RD LDR REC REG
631(e)
(LEFT) MSG STAT (AFD)
(LEFT) NEW STATUS
PEI BUS RD DR STA REG
EJ PORT PTR LEFT
642(e)
ZERO LEFT
632(e)
635(e)
640(e)
PEI BUS WRT LDR STA REG
DECR LEN REM
-1
PEI BUS RD LDR STA REG

FIG. 9D-2

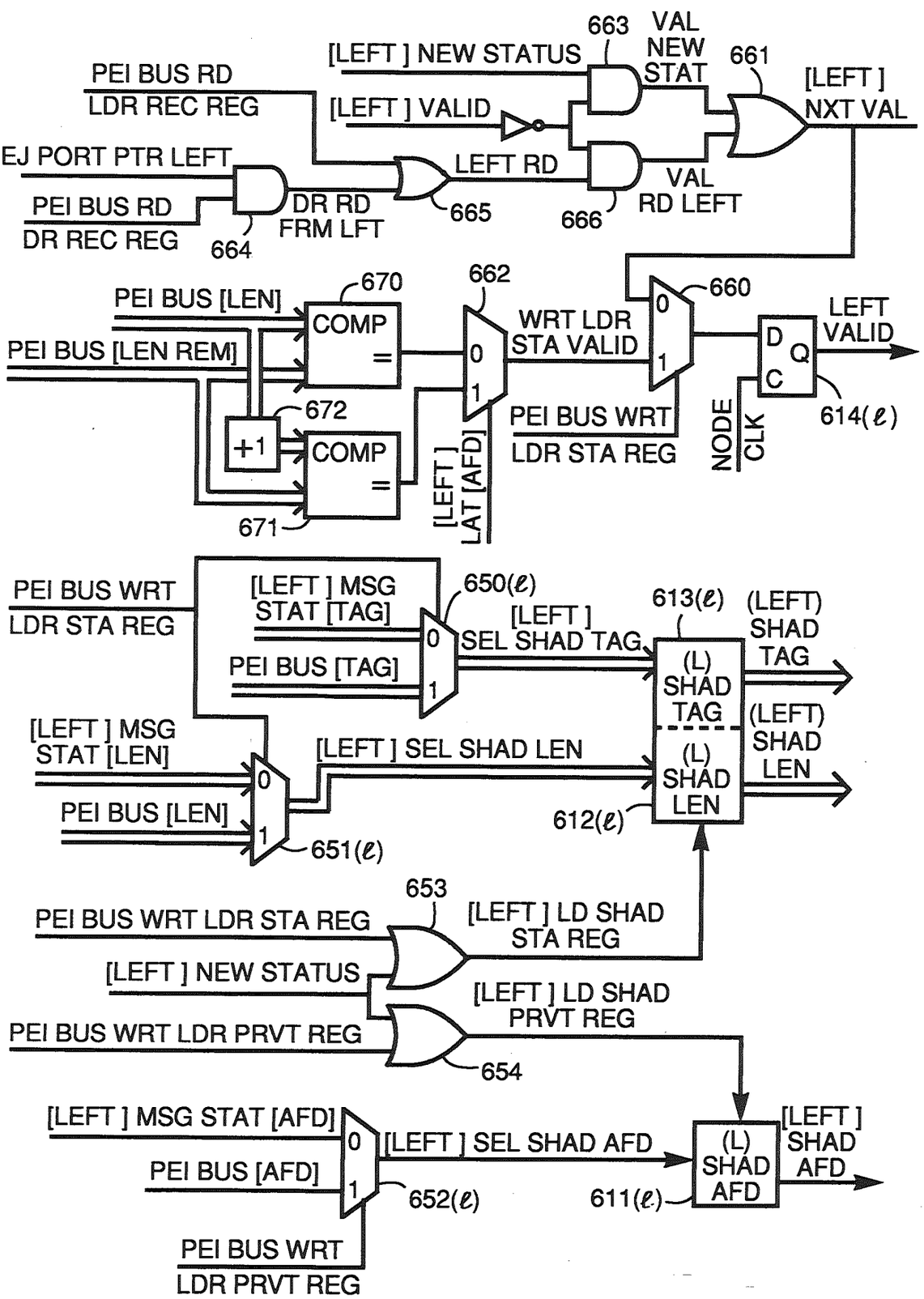

663
VAL NEW STAT
661
[LEFT] NEW STATUS
PEI BUS RD LDR REC REG
[LEFT] VALID
[LEFT] NXT VAL
EJ PORT PTR LEFT
LEFT RD
PEI BUS RD DR REC REG
DR RD FRM LFT
665
666
VAL RD LEFT
664
670
662
660
PEI BUS [LEN]
COMP =
WRT LDR STA VALID
LEFT VALID
PEI BUS [LEN REM]
672
+1
COMP =
PEI BUS WRT LDR STA REG
NODE CLK
614(ℓ)
671
[LEFT] LAT [AFD]
PEI BUS WRT LDR STA REG
[LEFT] MSG STAT [TAG]
650(ℓ)
613(ℓ)
(LEFT) SHAD TAG
[LEFT] SEL SHAD TAG
PEI BUS [TAG]
(L) SHAD TAG
(LEFT) SHAD LEN
[LEFT] MSG STAT [LEN]
[LEFT] SEL SHAD LEN
(L) SHAD LEN
PEI BUS [LEN]
612(ℓ)
651(ℓ)
653
PEI BUS WRT LDR STA REG
[LEFT] LD SHAD STA REG
[LEFT] NEW STATUS
[LEFT] LD SHAD PRVT REG
PEI BUS WRT LDR PRVT REG
654
[LEFT] MSG STAT [AFD]
[LEFT] SEL SHAD AFD
[LEFT] SHAD AFD
PEI BUS [AFD]
(L) SHAD AFD
652(ℓ)
611(ℓ)
PEI BUS WRT LDR PRVT REG

FIG. 9D-3

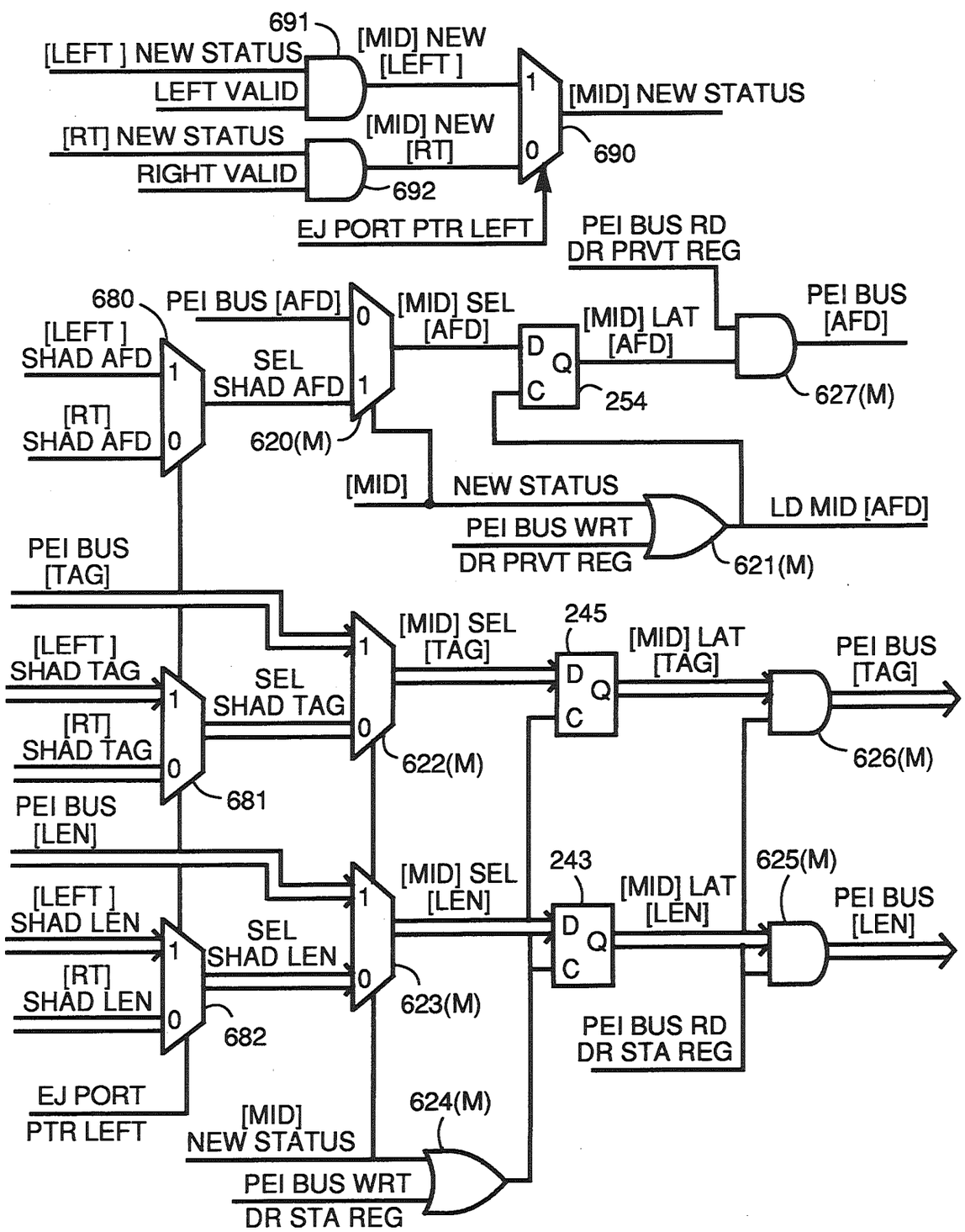
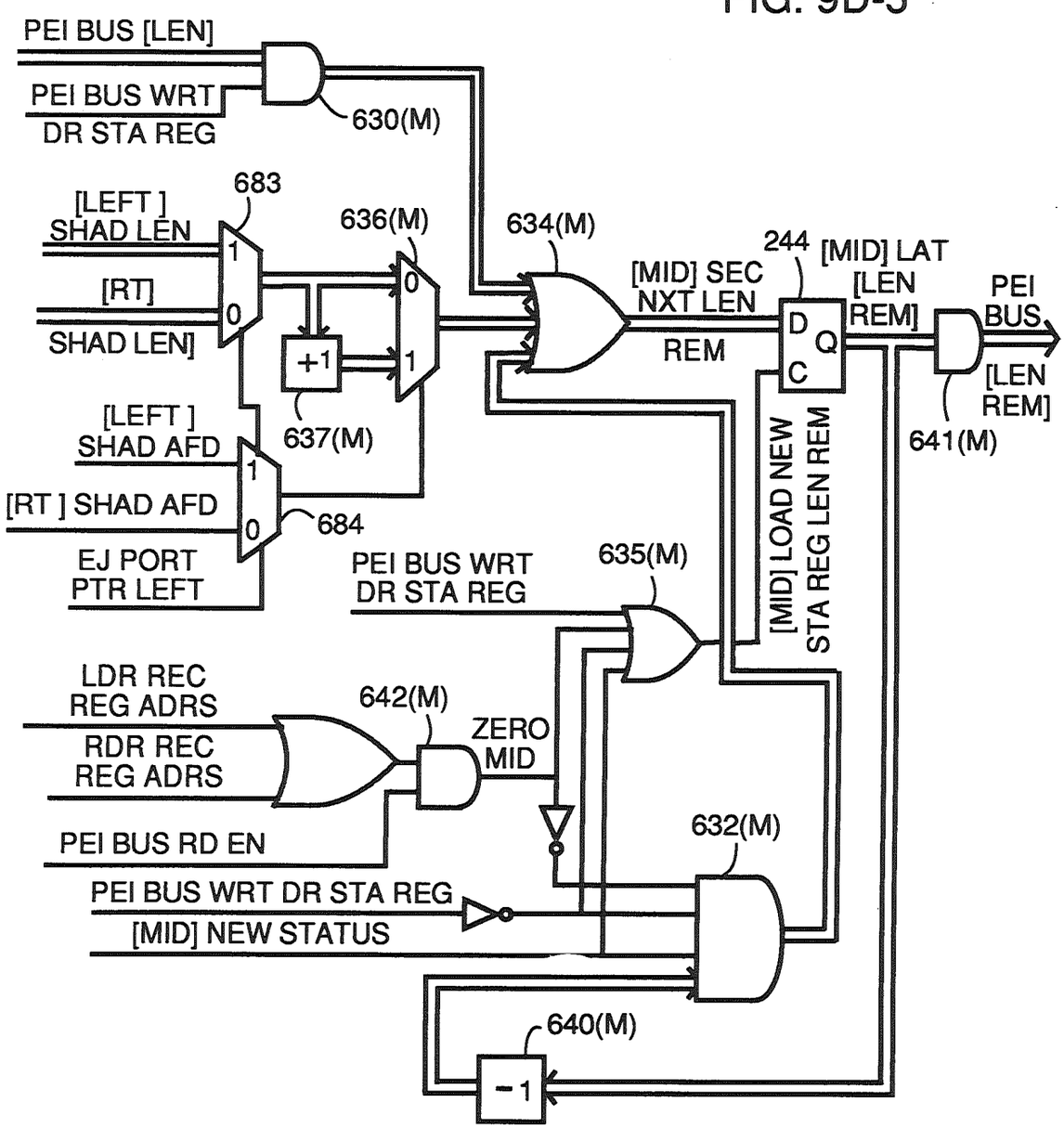

691
[MID] NEW
[LEFT]
[LEFT] NEW STATUS
LEFT VALID
[MID] NEW STATUS
[RT] NEW STATUS
[MID] NEW
[RT]
RIGHT VALID
690
692
EJ PORT PTR LEFT
PEI BUS RD
DR PRVT REG
680
PEI BUS [AFD]
[MID] SEL
[AFD]
[MID] LAT
[AFD]
PEI BUS
[AFD]
[LEFT]
SHAD AFD
SEL
SHAD AFD
[RT]
SHAD AFD
620(M)
254
627(M)
[MID]
NEW STATUS
LD MID [AFD]
PEI BUS WRT
DR PRVT REG
621(M)
PEI BUS
[TAG]
[MID] SEL
[TAG]
245
[MID] LAT
[TAG]
PEI BUS
[TAG]
[LEFT]
SHAD TAG
SEL
SHAD TAG
[RT]
SHAD TAG
622(M)
626(M)
681
PEI BUS
[LEN]
[MID] SEL
[LEN]
243
[MID] LAT
[LEN]
625(M)
PEI BUS
[LEN]
[LEFT]
SHAD LEN
SEL
SHAD LEN
[RT]
SHAD LEN
623(M)
682
PEI BUS RD
DR STA REG
EJ PORT
PTR LEFT
[MID]
NEW STATUS
624(M)
PEI BUS WRT
DR STA REG

FIG. 9D-4

FIG. 9D-5



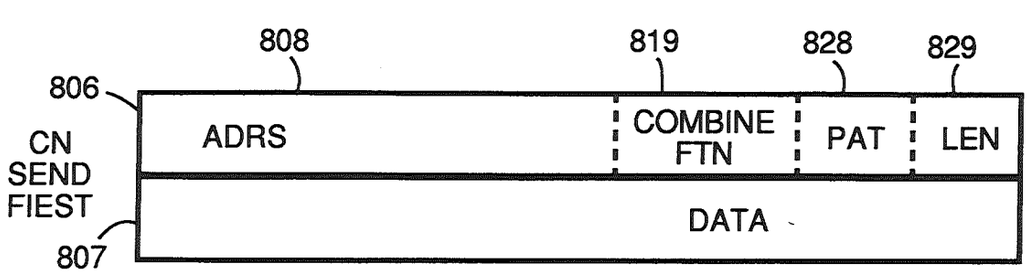


FIG. 10A-2

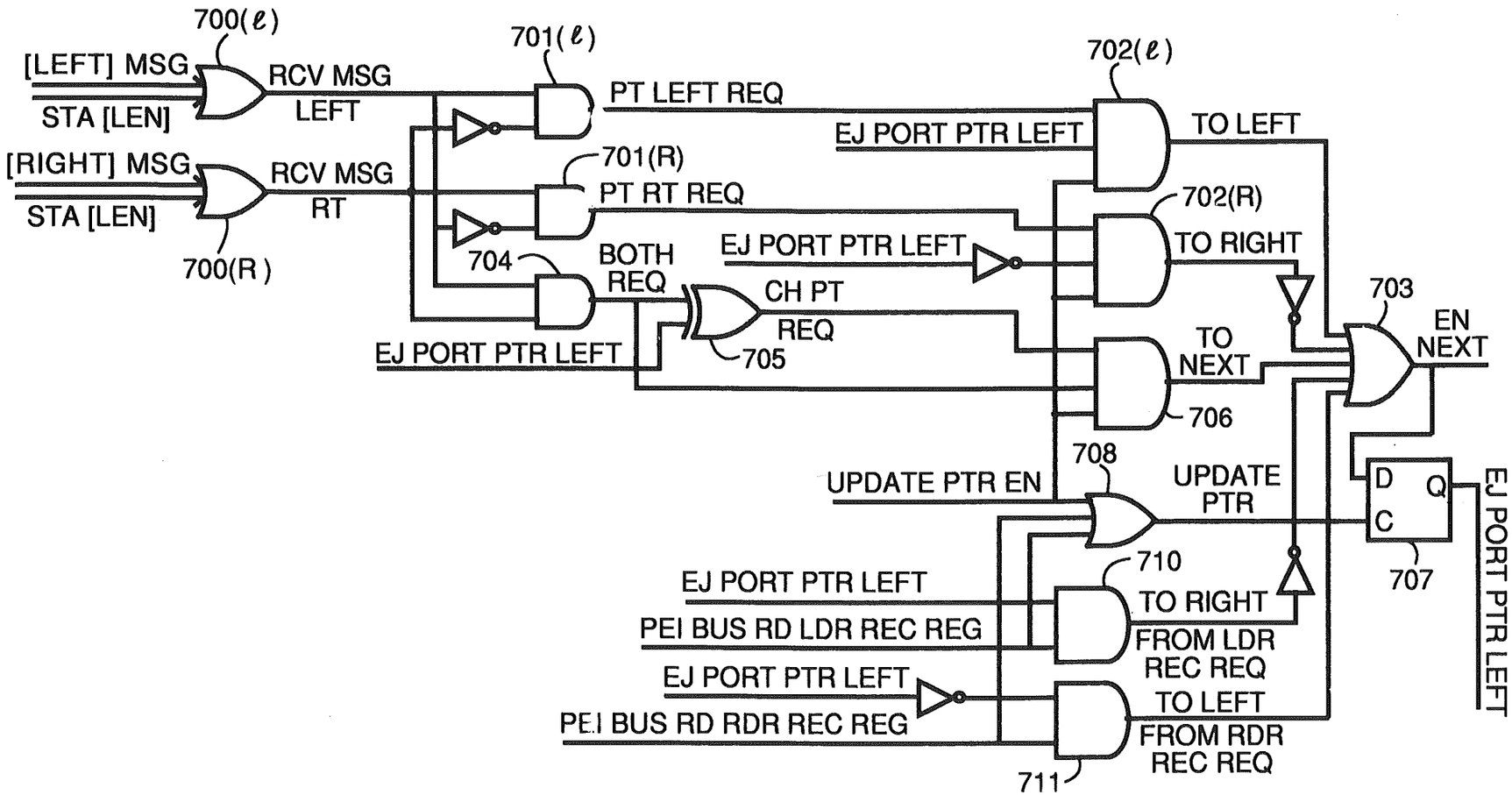
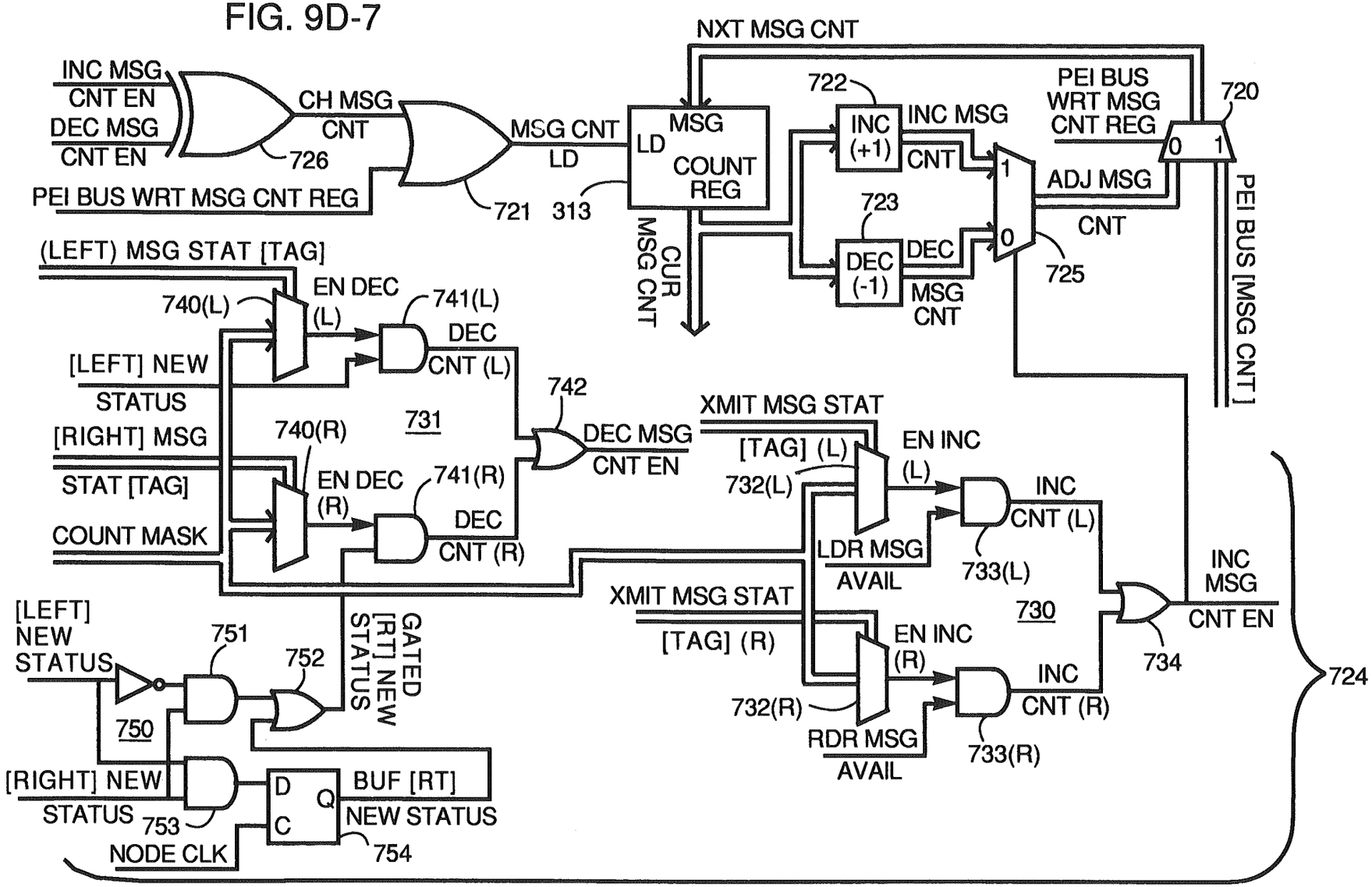

700(ℓ)
[LEFT] MSG
STA [LEN]
RCV MSG
LEFT
[RIGHT] MSG
STA [LEN]
RCV MSG
RT
700(R)
701(ℓ)
PT LEFT REQ
701(R)
PT RT REQ
704
BOTH
REQ
CH PT
REQ
705
EJ PORT PTR LEFT
EJ PORT PTR LEFT
702(ℓ)
TO LEFT
EJ PORT PTR LEFT
702(R)
TO RIGHT
TO
NEXT
706
703
EN
NEXT
UPDATE PTR EN
708
UPDATE
PTR
D
Q
C
707
EJ PORT PTR LEFT
EJ PORT PTR LEFT
PEI BUS RD LDR REC REG
710
TO RIGHT
FROM LDR
REC REQ
EJ PORT PTR LEFT
PEI BUS RD RDR REC REG
TO LEFT
FROM RDR
REC REQ
711

FIG. 9D-6

FIG. 9D-7


INC MSG
CNT EN
DEC MSG
CNT EN
CH MSG
CNT
726
PEI BUS WRT MSG CNT REG
721
MSG CNT
LD
313
MSG
LD
COUNT
REG
CUR
MSG CNT
NXT MSG CNT
722
INC
(+1)
INC MSG
CNT
723
DEC
(-1)
DEC
MSG
CNT
1
0
725
PEI BUS
WRT MSG
CNT REG
720
0
1
ADJ MSG
CNT
PEI BUS [MSG CNT]
(LEFT) MSG STAT [TAG]
740(L)
EN DEC
(L)
741(L)
DEC
CNT (L)
[LEFT] NEW
STATUS
[RIGHT] MSG
STAT [TAG]
COUNT MASK
740(R)
EN DEC
(R)
741(R)
DEC
CNT (R)
731
742
DEC MSG
CNT EN
XMIT MSG STAT
[TAG] (L)
732(L)
EN INC
(L)
INC
CNT (L)
LDR MSG
AVAIL
733(L)
XMIT MSG STAT
[TAG] (R)
732(R)
EN INC
(R)
INC
CNT (R)
RDR MSG
AVAIL
733(R)
730
INC
MSG
CNT EN
734
724
[LEFT]
NEW
STATUS
751
752
750
GATED
[RT] NEW
STATUS
[RIGHT] NEW
STATUS
753
D
C
Q
BUF [RT]
NEW STATUS
754
NODE CLK

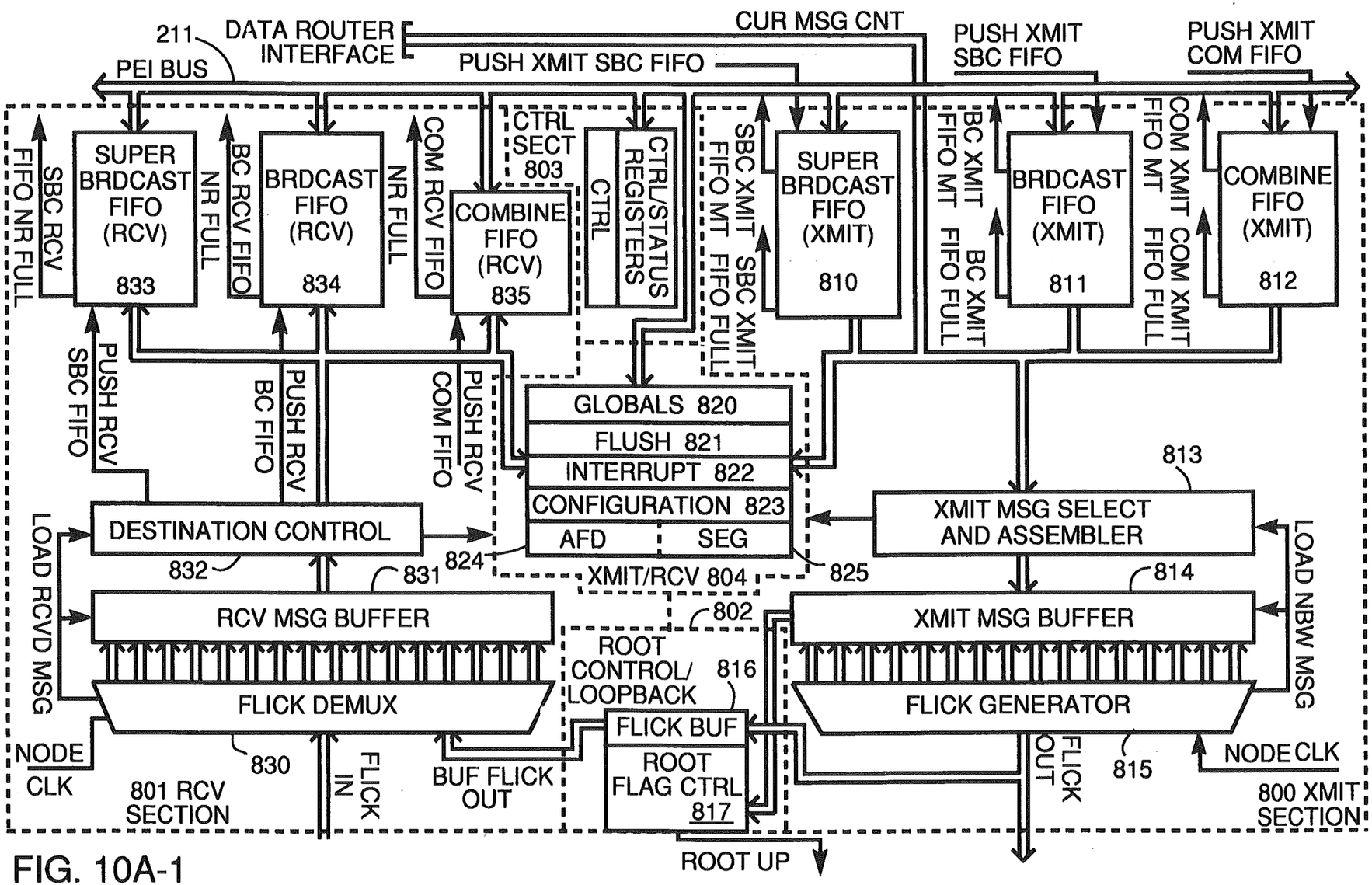

211
DATA ROUTER INTERFACE
PEI BUS
CUR MSG CNT
PUSH XMIT SBC FIFO
PUSH XMIT SBC FIFO
PUSH XMIT COM FIFO
SUPER BRDCAST FIFO (RCV) 833
BRDCAST FIFO (RCV) 834
COMBINE FIFO (RCV) 835
CTRL SECT 803
CTRL
CTRL/STATUS REGISTERS
SUPER BRDCAST FIFO (XMIT) 810
BRDCAST FIFO (XMIT) 811
COMBINE FIFO (XMIT) 812
SBC RCV FIFO NR FULL
BC RCV FIFO NR FULL
COM RCV FIFO NR FULL
SBC XMIT FIFO MT FIFO FULL
BC XMIT FIFO MT FIFO FULL
COM XMIT FIFO MT FIFO FULL
PUSH RCV SBC FIFO
PUSH RCV BC FIFO
PUSH RCV COM FIFO
GLOBALS 820
FLUSH 821
INTERRUPT 822
CONFIGURATION 823
AFD
SEG
813
XMIT MSG SELECT AND ASSEMBLER
DESTINATION CONTROL
832
831
824
XMIT/RCV 804
825
814
LOAD RCVD MSG
RCV MSG BUFFER
802
XMIT MSG BUFFER
LOAD NBW MSG
ROOT CONTROL/ LOOPBACK
816
FLICK DEMUX
FLICK BUF
FLICK GENERATOR
NODE CLK
830
FLICK IN
BUF FLICK OUT
ROOT FLAG CTRL 817
FLICK OUT
815
NODE CLK
801 RCV SECTION
800 XMIT SECTION
ROOT UP

FIG. 10A-1

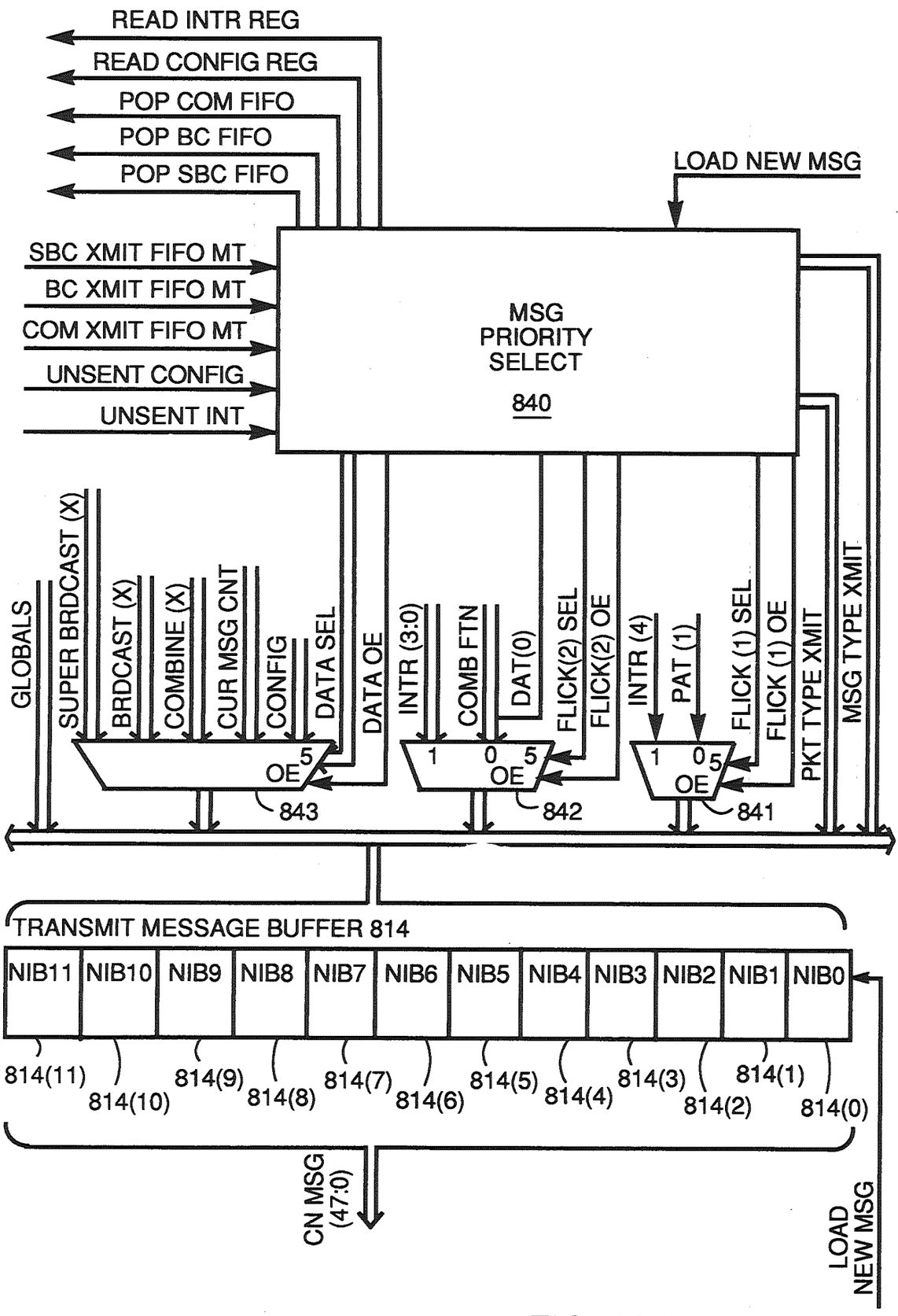
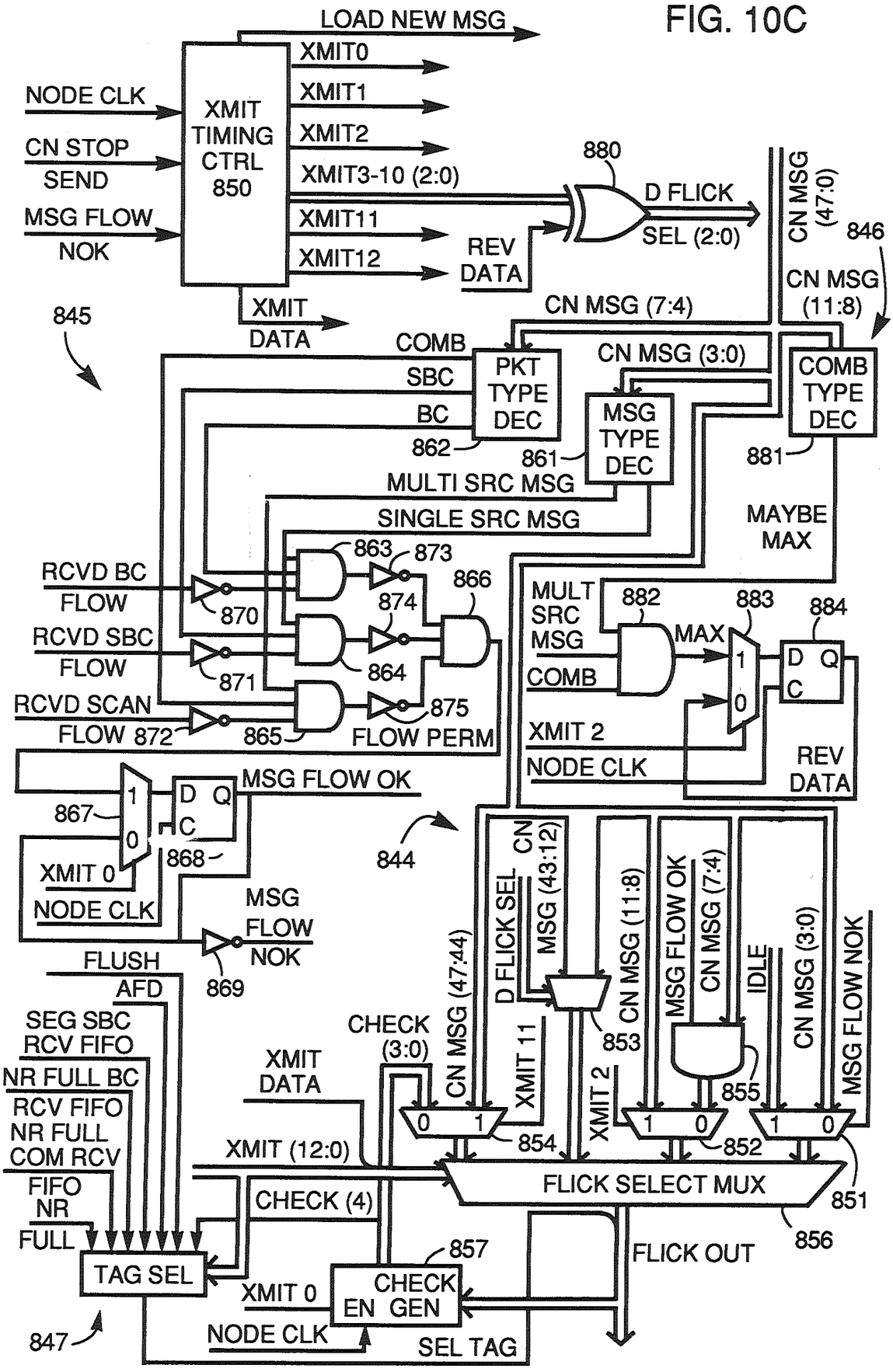

READ INTR REG
READ CONFIG REG
POP COM FIFO
POP BC FIFO
POP SBC FIFO
LOAD NEW MSG
SBC XMIT FIFO MT
BC XMIT FIFO MT
COM XMIT FIFO MT
UNSENT CONFIG
UNSENT INT
MSG PRIORITY SELECT
840
GLOBALS
SUPER BRDCAST (X)
BRDCAST (X)
COMBINE (X)
CUR MSG CNT
CONFIG
DATA SEL
DATA OE
INTR (3:0)
COMB FTN
DAT(0)
FLICK(2) SEL
FLICK(2) OE
INTR (4)
PAT (1)
FLICK (1) SEL
FLICK (1) OE
PKT TYPE XMIT
MSG TYPE XMIT
OE
843
842
841
TRANSMIT MESSAGE BUFFER 814
NIB11
NIB10
NIB9
NIB8
NIB7
NIB6
NIB5
NIB4
NIB3
NIB2
NIB1
NIB0
814(11)
814(10)
814(9)
814(8)
814(7)
814(6)
814(5)
814(4)
814(3)
814(2)
814(1)
814(0)
CN MSG (47:0)
LOAD NEW MSG

FIG. 10B

FIG. 10C


LOAD NEW MSG
XMIT0
XMIT1
XMIT2
XMIT3-10 (2:0)
XMIT11
XMIT12
NODE CLK
CN STOP SEND
MSG FLOW NOK
XMIT TIMING CTRL 850
880
D FLICK SEL (2:0)
REV DATA
CN MSG (47:0)
846
CN MSG (11:8)
CN MSG (7:4)
CN MSG (3:0)
XMIT DATA
845
COMB
SBC
BC
PKT TYPE DEC
862
MSG TYPE DEC
861
COMB TYPE DEC
881
MULTI SRC MSG
SINGLE SRC MSG
MAYBE MAX
863
873
866
RCVD BC FLOW
870
874
RCVD SBC FLOW
871
864
RCVD SCAN FLOW 872
865
875
FLOW PERM
MULT SRC MSG
COMB
882
MAX
883
884
D Q
C
XMIT 2
NODE CLK
REV DATA
MSG FLOW OK
867
868
XMIT 0
NODE CLK
844
MSG FLOW NOK
869
FLUSH
AFD
SEG SBC RCV FIFO
NR FULL BC
RCV FIFO NR FULL
COM RCV FIFO NR FULL
CHECK (3:0)
XMIT DATA
CN MSG (47:44)
D FLICK SEL
CN MSG (43:12)
XMIT 11
CN MSG (11:8)
XMIT 2
853
MSG FLOW OK
CN MSG (7:4)
IDLE
855
CN MSG (3:0)
MSG FLOW NOK
854
852
XMIT (12:0)
FLICK SELECT MUX
851
856
CHECK (4)
FLICK OUT
857
TAG SEL
CHECK EN GEN
XMIT 0
NODE CLK
SEL TAG
847

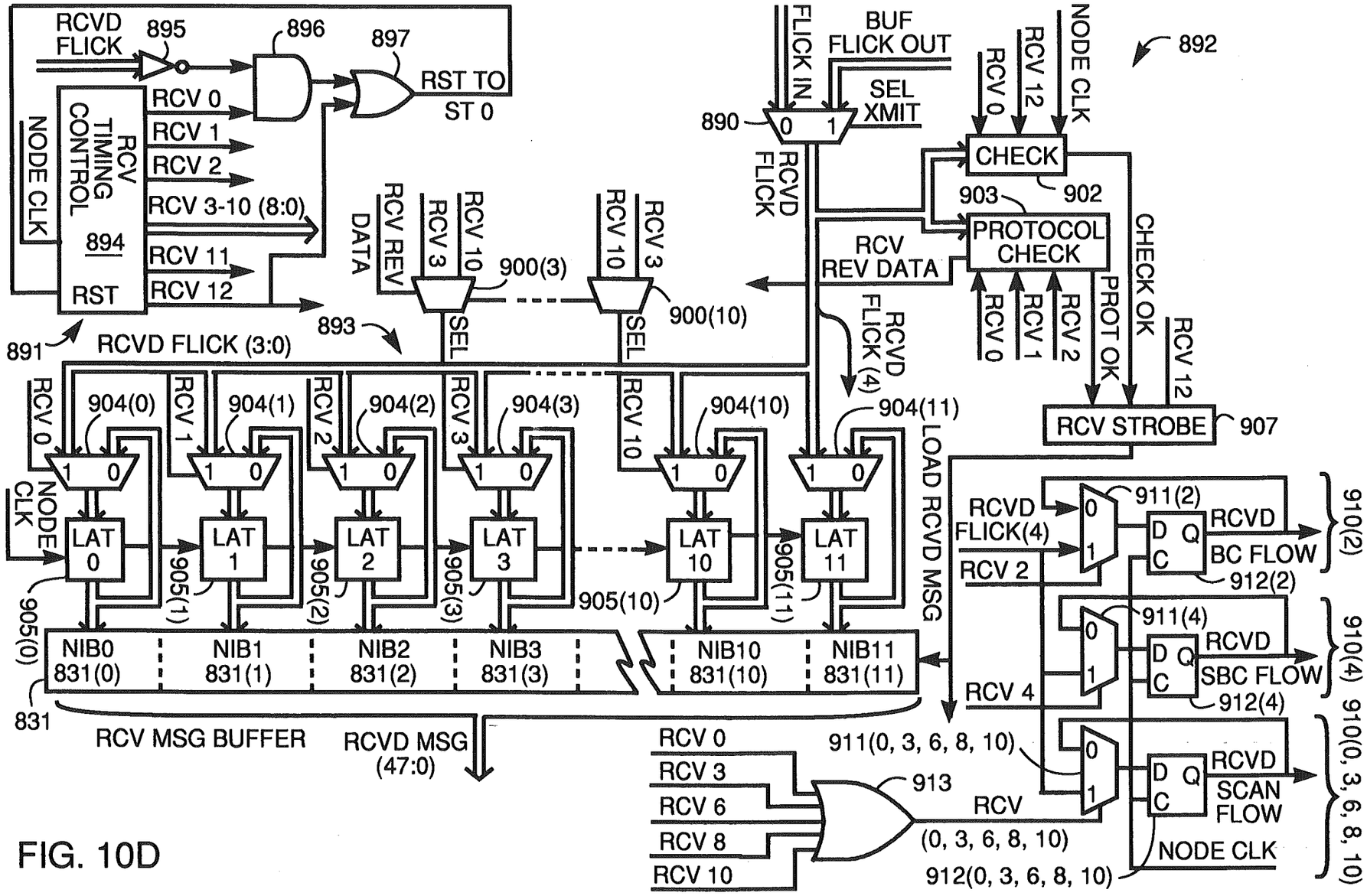
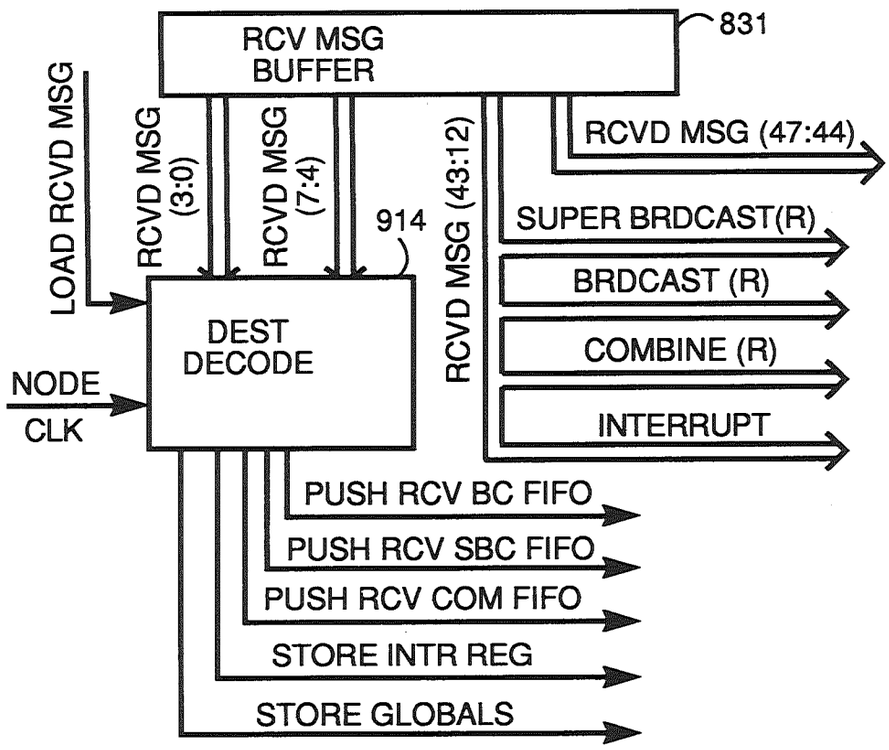

RCVD FLICK
895
896
897
RST TO ST 0
RCV 0
RCV 1
RCV 2
RCV 3-10 (8:0)
RCV 11
RCV 12
RST
NODE CLK
RCV TIMING CONTROL
894
891
RCVD FLICK (3:0)
893
RCV REV DATA
RCV 3
RCV 10
900(3)
900(10)
SEL
FLICK IN
BUF FLICK OUT
SEL XMIT
890
RCVD FLICK
RCV REV DATA
RCVD FLICK (4)
892
CHECK
902
903
PROTOCOL CHECK
PROT OK
CHECK OK
RCV STROBE
907
LOAD RCVD MSG
904(0)
904(1)
904(2)
904(3)
904(10)
904(11)
LAT 0
LAT 1
LAT 2
LAT 3
LAT 10
LAT 11
905(0)
905(1)
905(2)
905(3)
905(10)
905(11)
NIB0 831(0)
NIB1 831(1)
NIB2 831(2)
NIB3 831(3)
NIB10 831(10)
NIB11 831(11)
831
RCV MSG BUFFER
RCVD MSG (47:0)
RCVD FLICK(4)
RCV 2
911(2)
RCVD
BC FLOW
912(2)
910(2)
RCV 4
911(4)
SBC FLOW
912(4)
910(4)
911(0, 3, 6, 8, 10)
SCAN FLOW
912(0, 3, 6, 8, 10)
910(0, 3, 6, 8, 10)
RCV 0
RCV 3
RCV 6
RCV 8
RCV 10
913
RCV
(0, 3, 6, 8, 10)
D
Q
C

FIG. 10D



CONTROL NETWORK
INTERFACE RCV SECTION
DESTINATION CONTROL

FIG. 10E

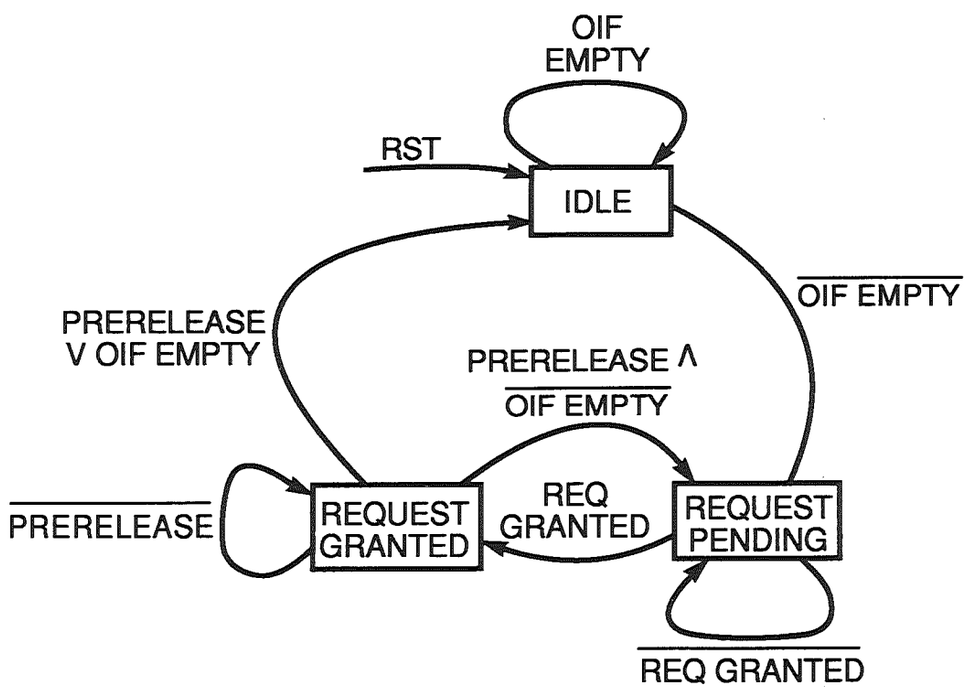


FIG. 11B-3A

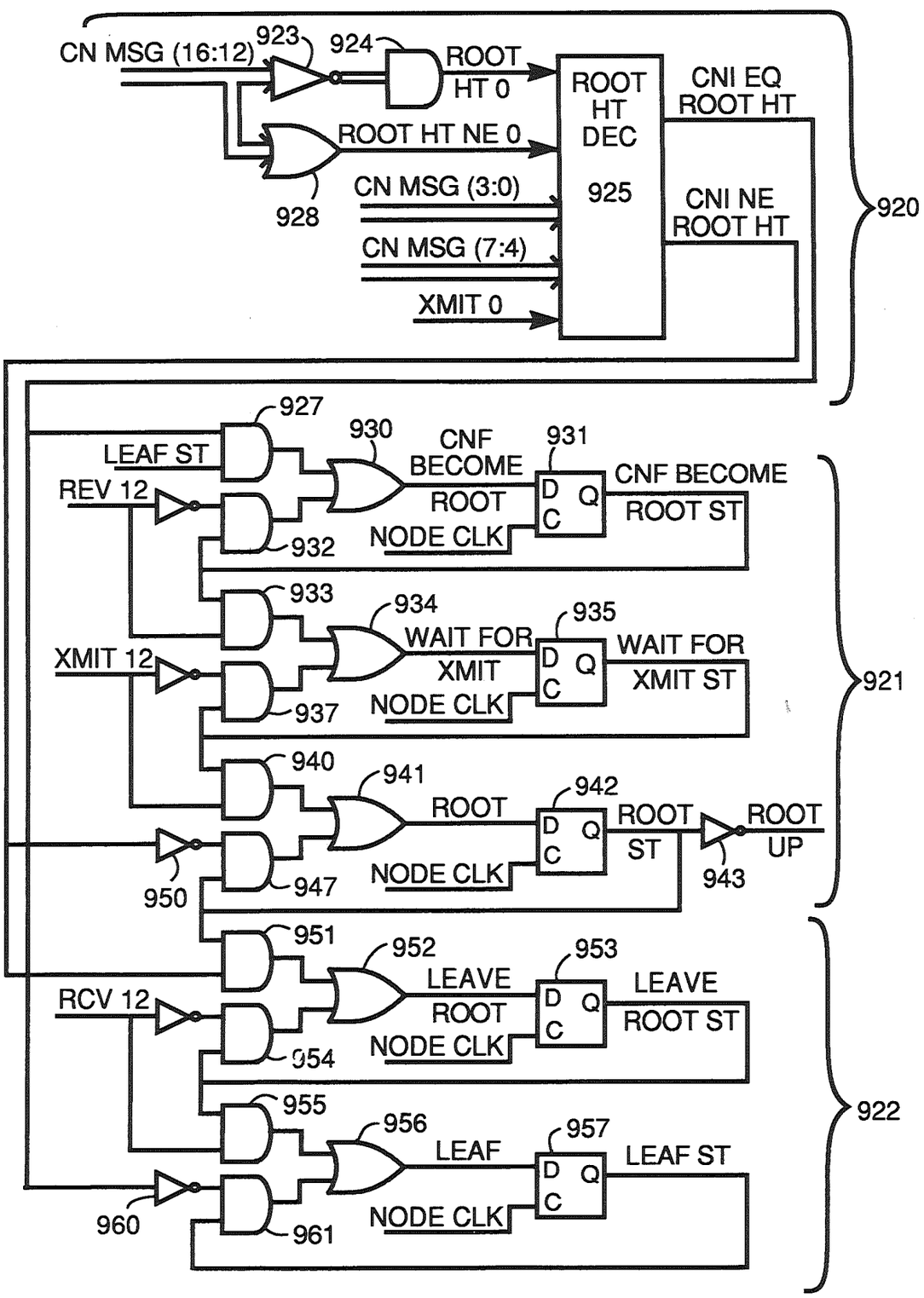

CN MSG (16:12)
923
924
ROOT HT 0
ROOT HT NE 0
928
CN MSG (3:0)
CN MSG (7:4)
XMIT 0
ROOT HT DEC
925
CNI EQ ROOT HT
CNI NE ROOT HT
920
927
930
931
LEAF ST
REV 12
CNF BECOME ROOT NODE CLK
D Q C
CNF BECOME ROOT ST
932
933
934
935
XMIT 12
WAIT FOR XMIT NODE CLK
WAIT FOR XMIT ST
937
921
940
941
942
ROOT NODE CLK
ROOT ST
ROOT UP
943
950
947
951
952
953
RCV 12
LEAVE ROOT NODE CLK
LEAVE ROOT ST
954
955
956
957
LEAF NODE CLK
LEAF ST
960
961
922

FIG. 10F

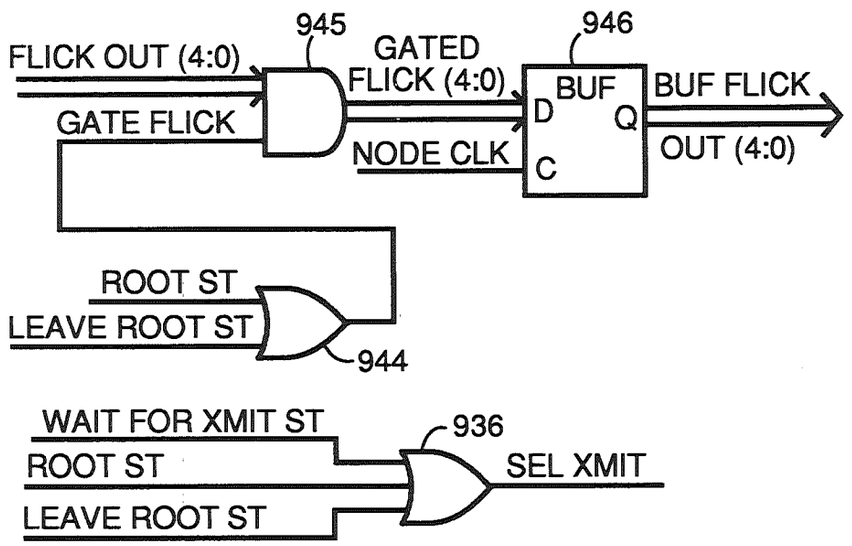


FIG. 10G

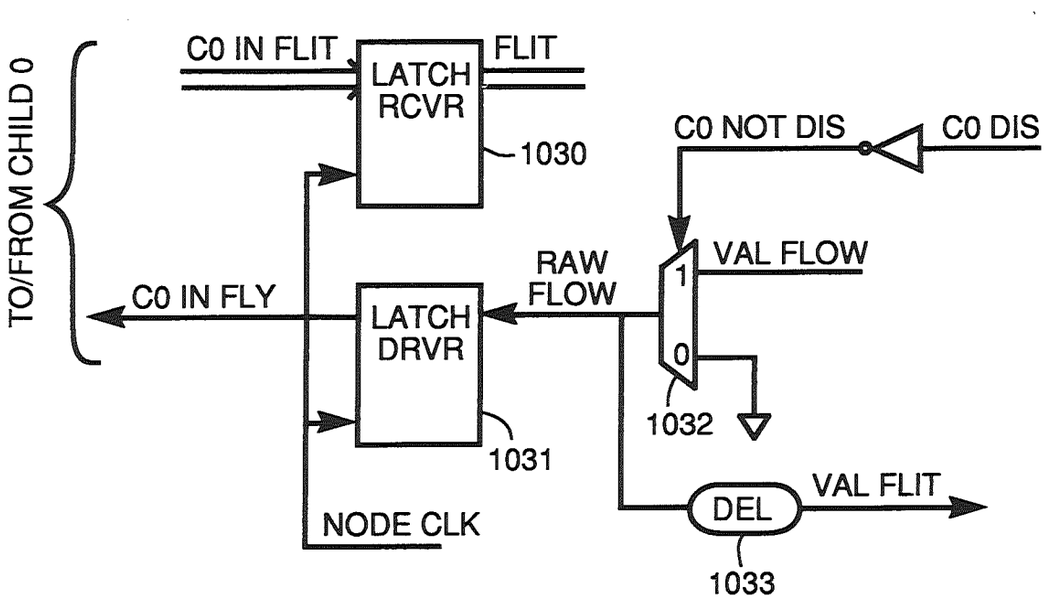


FIG. 11B-1

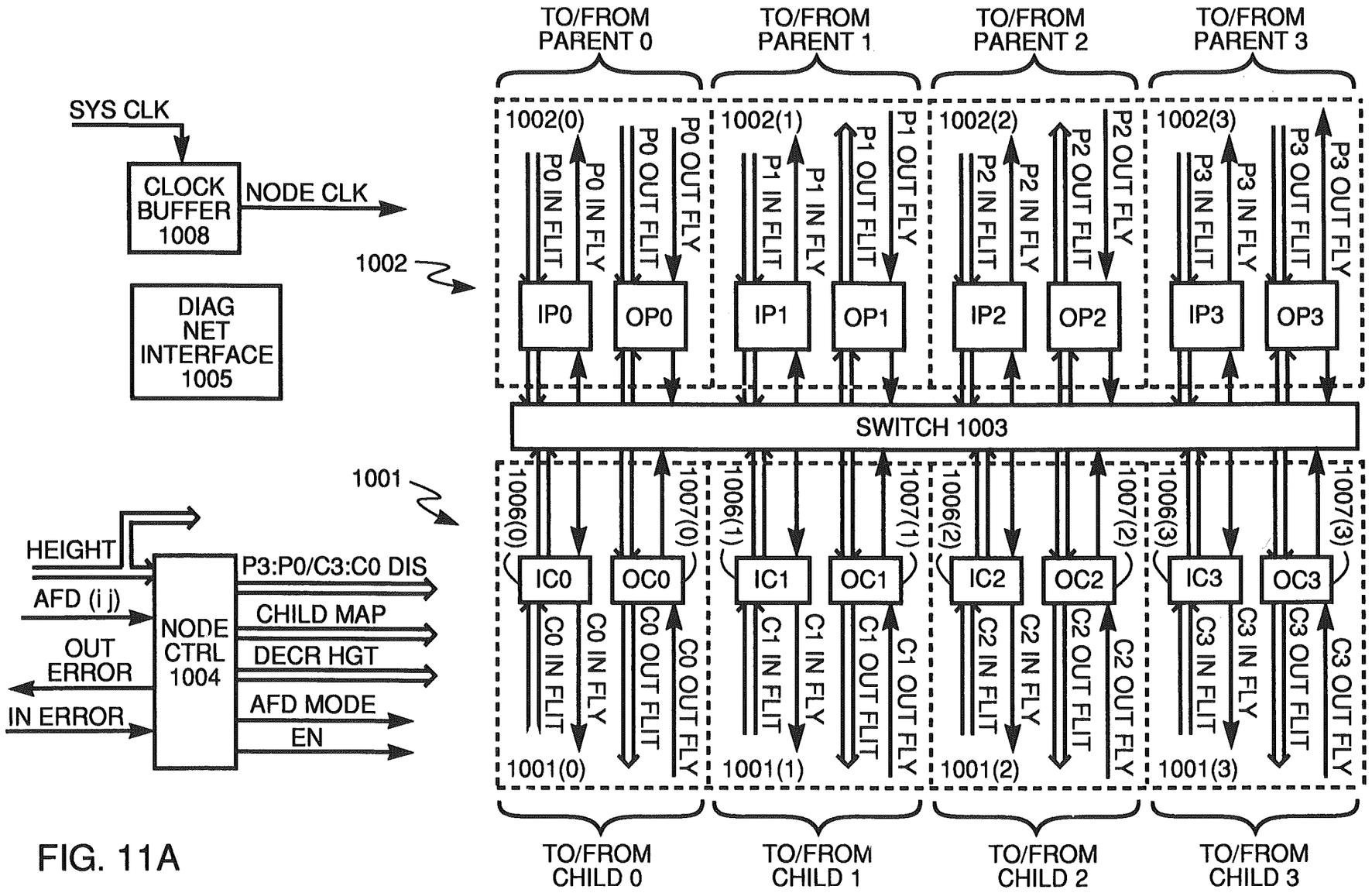

SYS CLK
CLOCK BUFFER 1008
NODE CLK
1002
DIAG NET INTERFACE 1005
1001
HEIGHT
AFD (i j)
OUT ERROR
IN ERROR
NODE CTRL 1004
P3:P0/C3:C0 DIS
CHILD MAP
DECR HGT
AFD MODE
EN
TO/FROM PARENT 0
TO/FROM PARENT 1
TO/FROM PARENT 2
TO/FROM PARENT 3
1002(0)
1002(1)
1002(2)
1002(3)
P0 IN FLIT
P0 IN FLY
P0 OUT FLIT
P0 OUT FLY
P1 IN FLIT
P1 IN FLY
P1 OUT FLIT
P1 OUT FLY
P2 IN FLIT
P2 IN FLY
P2 OUT FLIT
P2 OUT FLY
P3 IN FLIT
P3 IN FLY
P3 OUT FLIT
P3 OUT FLY
IP0
OP0
IP1
OP1
IP2
OP2
IP3
OP3
SWITCH 1003
1006(0)
1007(0)
1006(1)
1007(1)
1006(2)
1007(2)
1006(3)
1007(3)
IC0
OC0
IC1
OC1
IC2
OC2
IC3
OC3
C0 IN FLIT
C0 IN FLY
C0 OUT FLIT
C0 OUT FLY
C1 IN FLIT
C1 IN FLY
C1 OUT FLIT
C1 OUT FLY
C2 IN FLIT
C2 IN FLY
C2 OUT FLIT
C2 OUT FLY
C3 IN FLIT
C3 IN FLY
C3 OUT FLIT
C3 OUT FLY
1001(0)
1001(1)
1001(2)
1001(3)
TO/FROM CHILD 0
TO/FROM CHILD 1
TO/FROM CHILD 2
TO/FROM CHILD 3

FIG. 11A

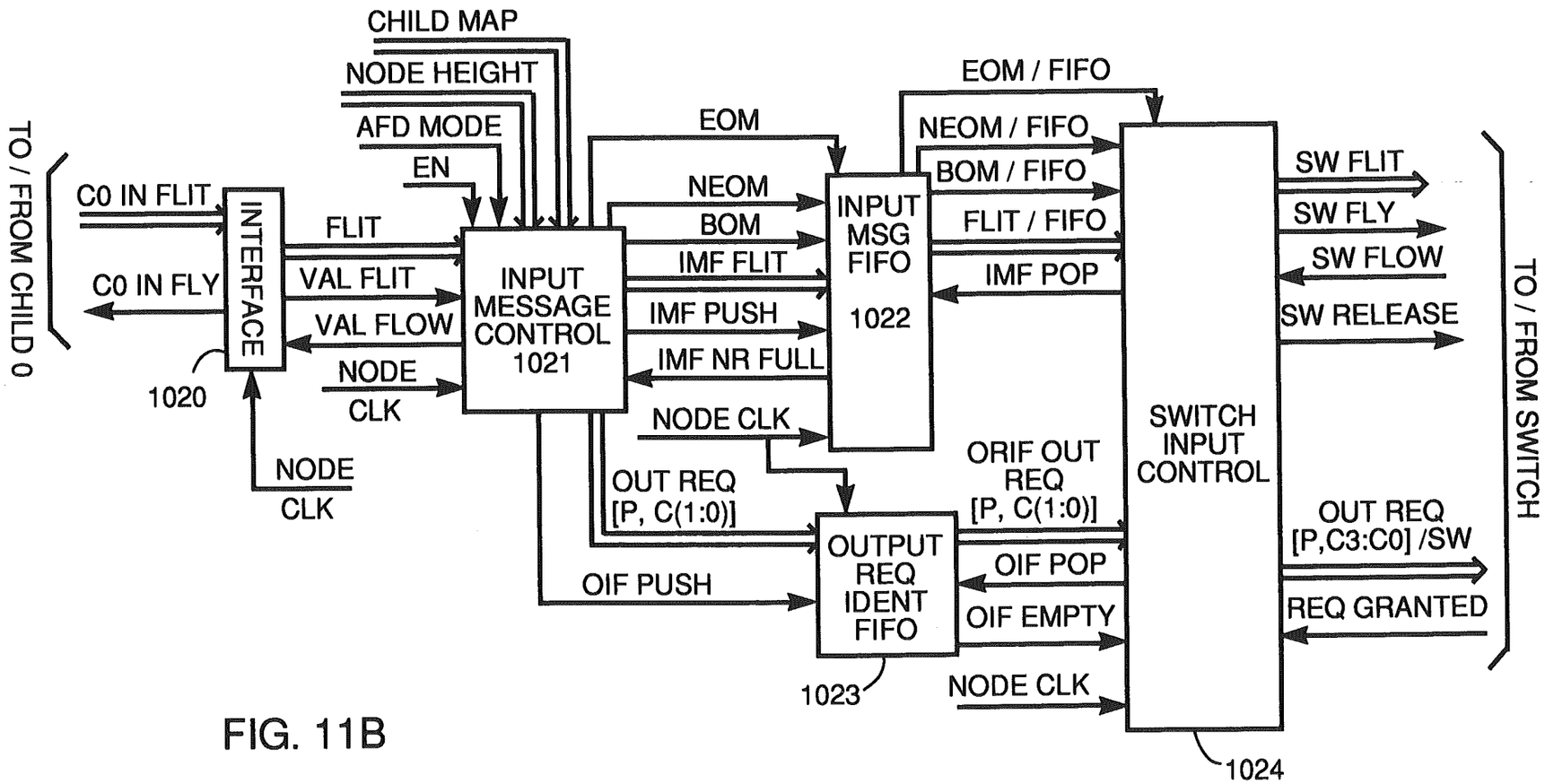

CHILD MAP
NODE HEIGHT
AFD MODE
EN
EOM
EOM / FIFO
NEOM / FIFO
BOM / FIFO
FLIT / FIFO
IMF POP
SW FLIT
SW FLY
SW FLOW
SW RELEASE
TO / FROM CHILD 0
C0 IN FLIT
C0 IN FLY
INTERFACE
1020
FLIT
VAL FLIT
VAL FLOW
NODE CLK
INPUT MESSAGE CONTROL 1021
NEOM
BOM
IMF FLIT
IMF PUSH
IMF NR FULL
NODE CLK
INPUT MSG FIFO 1022
SWITCH INPUT CONTROL
TO / FROM SWITCH
NODE CLK
OUT REQ [P, C(1:0)]
ORIF OUT REQ [P, C(1:0)]
OUT REQ [P,C3:C0] /SW
OIF POP
OIF PUSH
OIF EMPTY
REQ GRANTED
OUTPUT REQ IDENT FIFO
1023
NODE CLK
1024

FIG. 11B

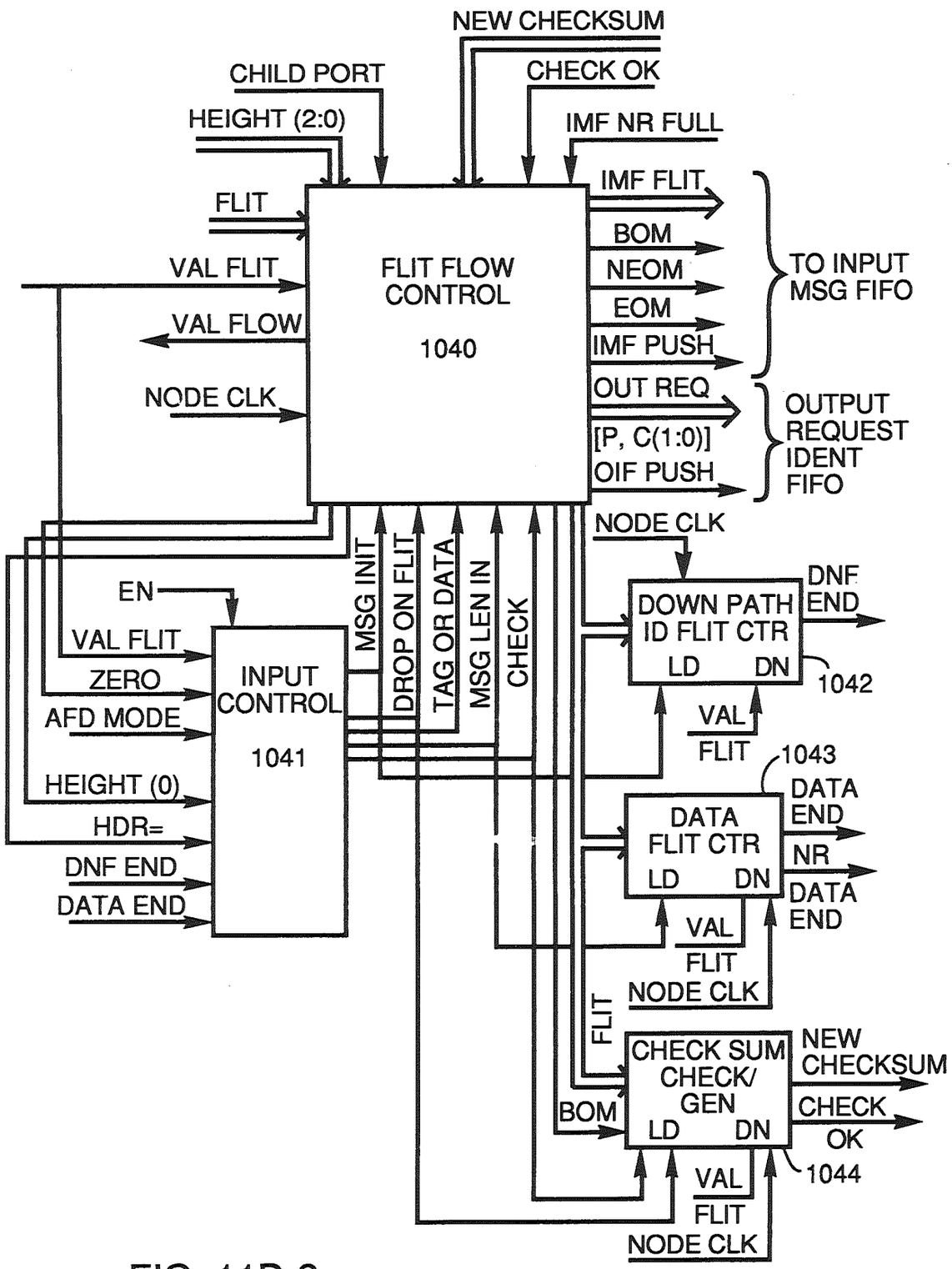

NEW CHECKSUM
CHILD PORT
CHECK OK
HEIGHT (2:0)
IMF NR FULL
IMF FLIT
FLIT
BOM
VAL FLIT
FLIT FLOW CONTROL
1040
NEOM
TO INPUT MSG FIFO
VAL FLOW
EOM
IMF PUSH
NODE CLK
OUT REQ
OUTPUT REQUEST IDENT FIFO
[P, C(1:0)]
OIF PUSH
NODE CLK
EN
MSG INIT
DROP ON FLIT
TAG OR DATA
MSG LEN IN
CHECK
DNF END
DOWN PATH ID FLIT CTR
LD
DN
1042
VAL FLIT
VAL FLIT
ZERO
INPUT CONTROL
1041
AFD MODE
1043
DATA END
DATA FLIT CTR
LD
DN
NR
DATA END
HEIGHT (0)
HDR=
VAL FLIT
NODE CLK
DNF END
DATA END
FLIT
CHECK SUM CHECK/ GEN
NEW CHECKSUM
BOM
LD
DN
CHECK OK
1044
VAL FLIT
NODE CLK

FIG. 11B-2

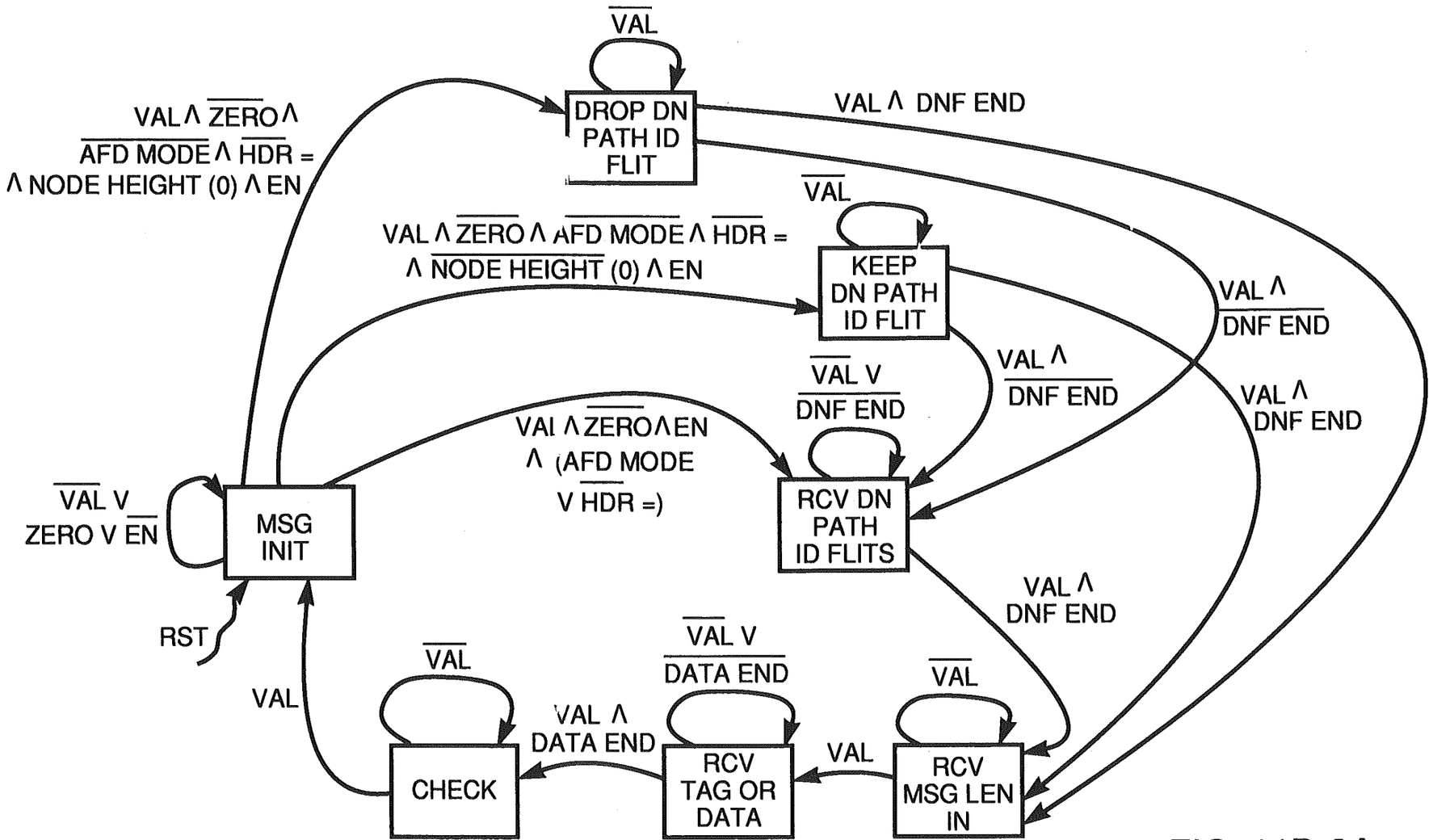
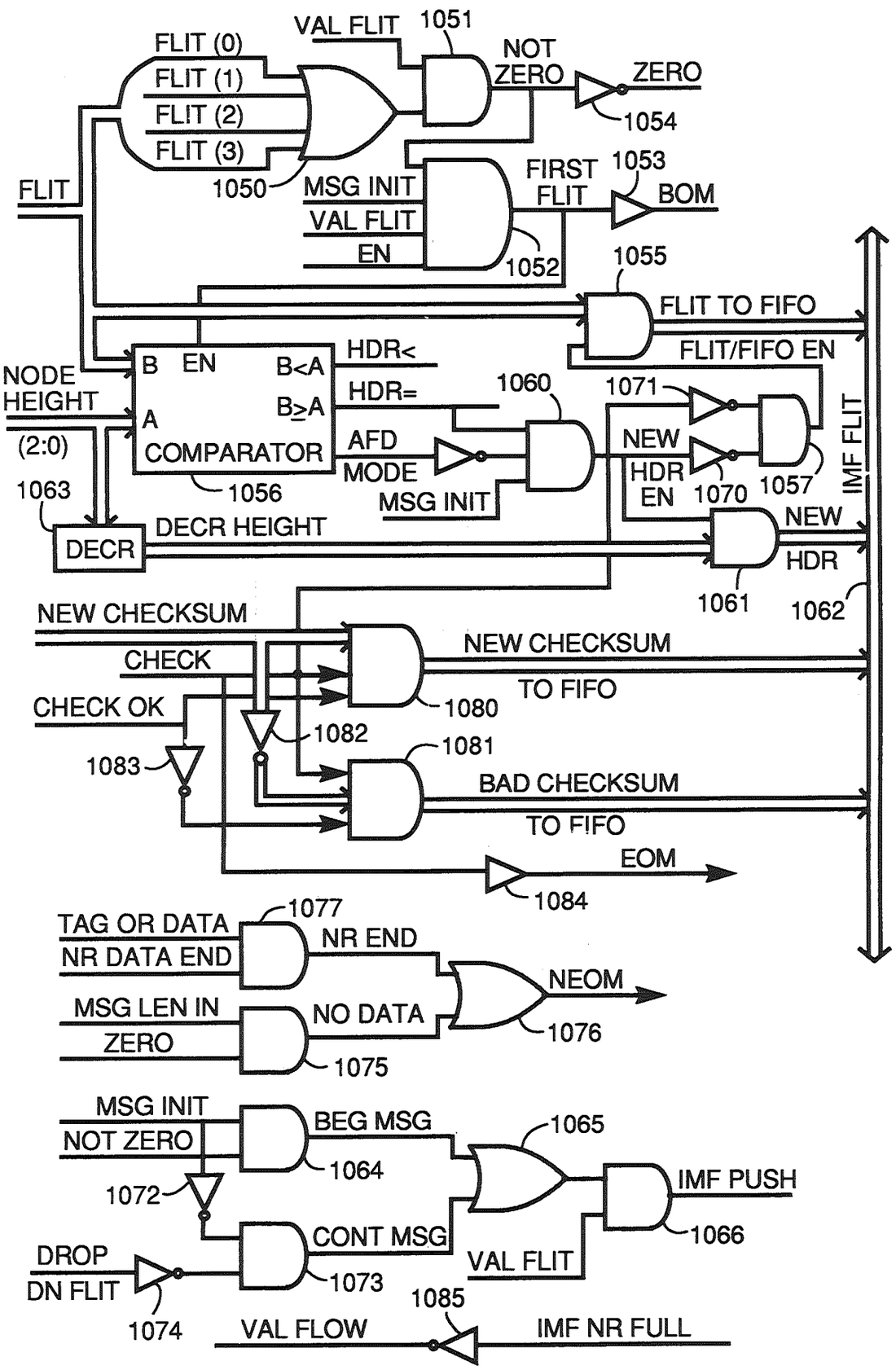

VAL
DROP DN PATH ID FLIT
VAL ∧ DNF END
VAL ∧ ZERO ∧ AFD MODE ∧ HDR = ∧ NODE HEIGHT (0) ∧ EN
VAL
KEEP DN PATH ID FLIT
VAL ∧ ZERO ∧ AFD MODE ∧ HDR = ∧ NODE HEIGHT (0) ∧ EN
VAL ∧ DNF END
VAL ∧ DNF END
VAL V DNF END
VAL ∧ DNF END
VAL ∧ ZERO ∧ EN ∧ (AFD MODE V HDR =)
VAL V ZERO V EN
MSG INIT
RCV DN PATH ID FLITS
VAL ∧ DNF END
RST
VAL
VAL V DATA END
VAL
VAL
VAL ∧ DATA END
CHECK
RCV TAG OR DATA
VAL
RCV MSG LEN IN

FIG. 11B-2A

FIG. 11B-2B


VAL FLIT
1051
FLIT (0)
FLIT (1)
FLIT (2)
FLIT (3)
NOT ZERO
ZERO
1054
1050
FLIT
MSG INIT
VAL FLIT
EN
FIRST FLIT
1053
BOM
1052
1055
FLIT TO FIFO
FLIT/FIFO EN
NODE HEIGHT
(2:0)
B
EN
A
B<A
B≥A
COMPARATOR
1056
HDR<
HDR=
AFD
MODE
MSG INIT
1060
1071
NEW HDR EN
1070
1057
IMF FLIT
1063
DECR
DECR HEIGHT
NEW HDR
1061
1062
NEW CHECKSUM
CHECK
CHECK OK
1083
1082
1080
NEW CHECKSUM TO FIFO
1081
BAD CHECKSUM TO FIFO
EOM
1084
TAG OR DATA
NR DATA END
1077
NR END
MSG LEN IN
ZERO
NO DATA
1075
NEOM
1076
MSG INIT
NOT ZERO
1072
BEG MSG
1064
1065
CONT MSG
1073
IMF PUSH
1066
VAL FLIT
DROP DN FLIT
1074
1085
VAL FLOW
IMF NR FULL

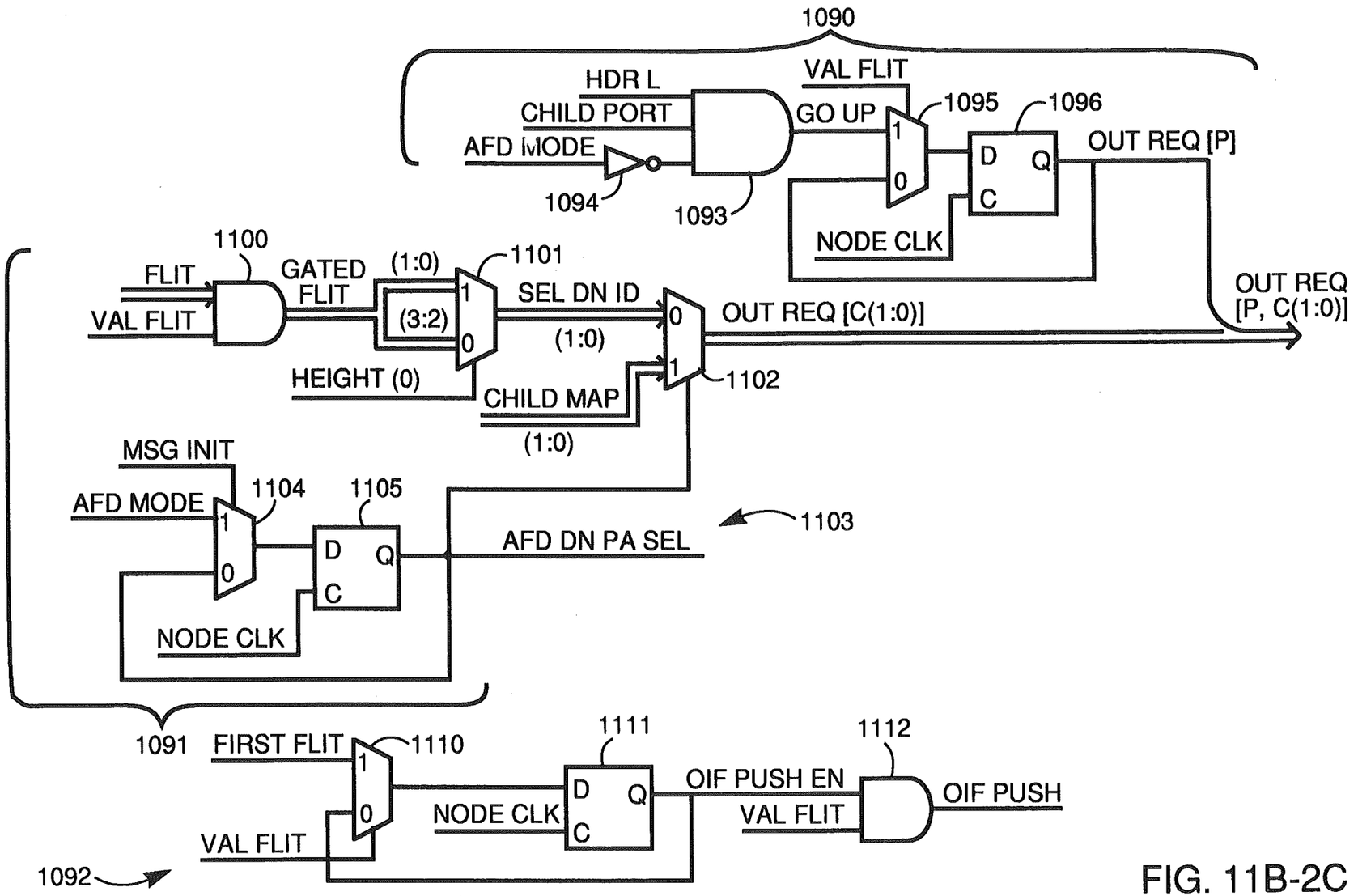

1090
HDR L
CHILD PORT
AFD MODE
1094
1093
VAL FLIT
GO UP
1095
1096
1
0
D
Q
C
OUT REQ [P]
NODE CLK
1100
FLIT
VAL FLIT
GATED FLIT
(1:0)
(3:2)
1101
SEL DN ID
(1:0)
OUT REQ [C(1:0)]
OUT REQ [P, C(1:0)]
HEIGHT (0)
CHILD MAP
(1:0)
1102
MSG INIT
AFD MODE
1104
1105
1103
AFD DN PA SEL
NODE CLK
1091
FIRST FLIT
1110
1111
1112
NODE CLK
OIF PUSH EN
OIF PUSH
VAL FLIT
VAL FLIT
1092

FIG. 11B-2C

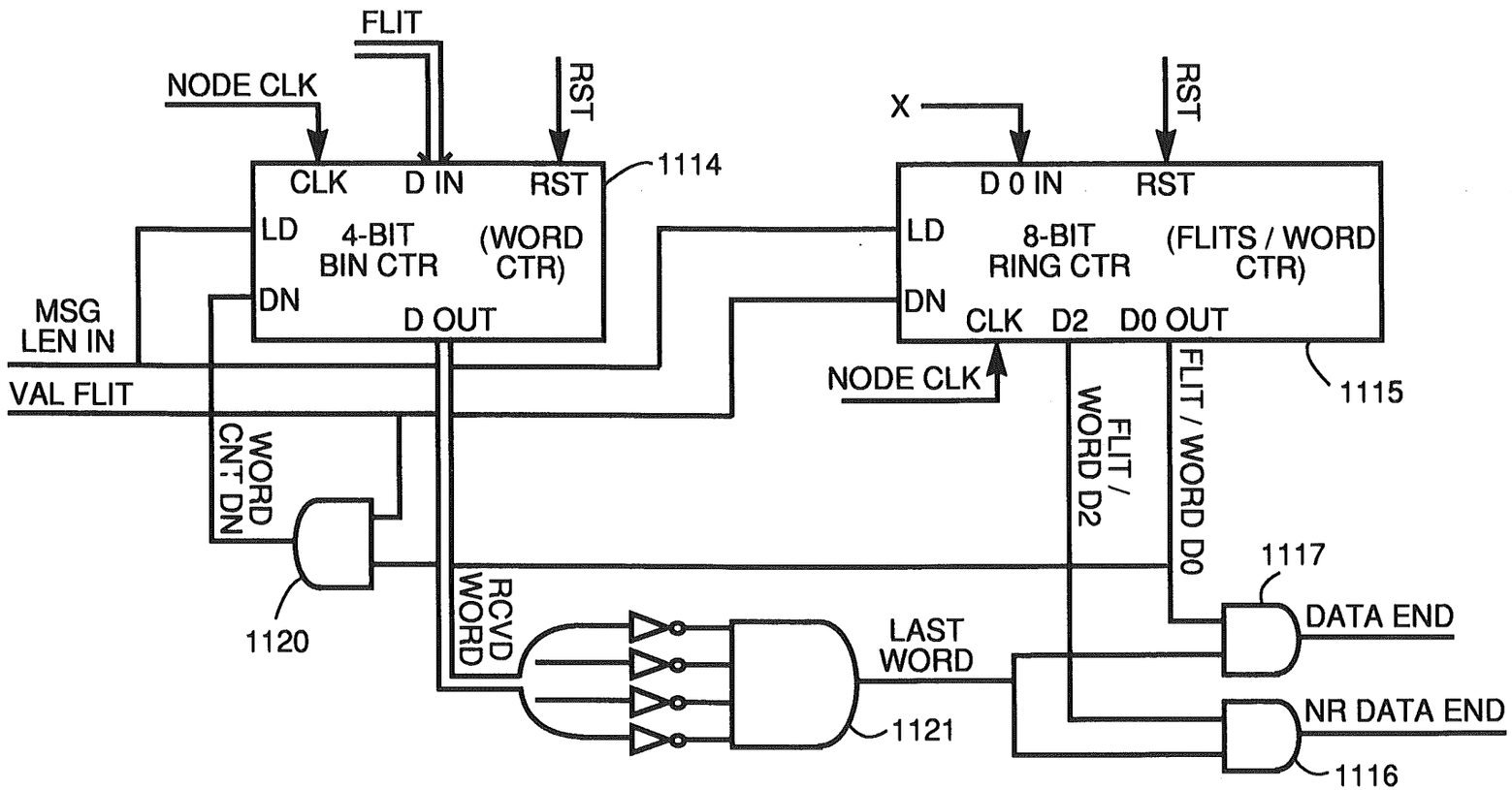

FLIT
NODE CLK
RST
CLK
D IN
RST
1114
LD
4-BIT
BIN CTR
(WORD
CTR)
DN
D OUT
MSG
LEN IN
VAL FLIT
WORD CNT DN
1120
RCVD WORD
X
RST
D 0 IN
RST
LD
8-BIT
RING CTR
(FLITS / WORD
CTR)
DN
CLK
D2
D0 OUT
NODE CLK
1115
FLIT / WORD D2
FLIT / WORD D0
1117
DATA END
LAST WORD
NR DATA END
1121
1116

FIG. 11B-2D

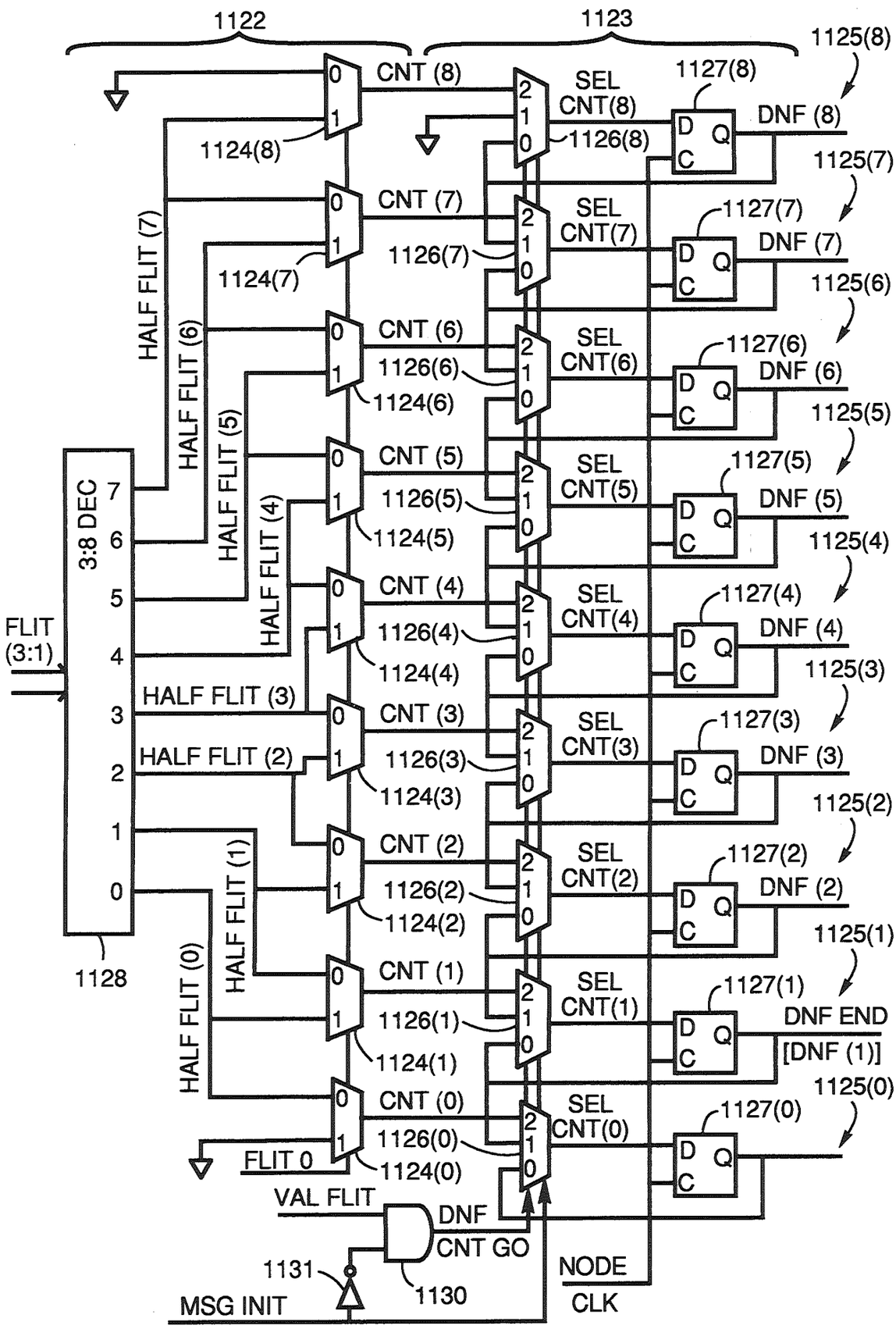

1122
1123
1125(8)
CNT (8)
SEL CNT(8)
1127(8)
DNF (8)
1124(8)
1126(8)
1125(7)
CNT (7)
SEL CNT(7)
1127(7)
DNF (7)
1124(7)
1126(7)
1125(6)
CNT (6)
SEL CNT(6)
1127(6)
DNF (6)
1126(6)
1124(6)
1125(5)
CNT (5)
SEL CNT(5)
1127(5)
DNF (5)
1126(5)
1124(5)
1125(4)
CNT (4)
SEL CNT(4)
1127(4)
DNF (4)
1126(4)
1124(4)
1125(3)
CNT (3)
SEL CNT(3)
1127(3)
DNF (3)
1126(3)
1124(3)
1125(2)
CNT (2)
SEL CNT(2)
1127(2)
DNF (2)
1126(2)
1124(2)
1125(1)
CNT (1)
SEL CNT(1)
1127(1)
DNF END
[DNF (1)]
1126(1)
1124(1)
1125(0)
CNT (0)
SEL CNT(0)
1127(0)
1126(0)
1124(0)
FLIT 0
VAL FLIT
DNF
CNT GO
1131
1130
MSG INIT
NODE
CLK
3:8 DEC
1128
FLIT (3:1)
HALF FLIT (7)
HALF FLIT (6)
HALF FLIT (5)
HALF FLIT (4)
HALF FLIT (3)
HALF FLIT (2)
HALF FLIT (1)
HALF FLIT (0)

FIG. 11B-2E

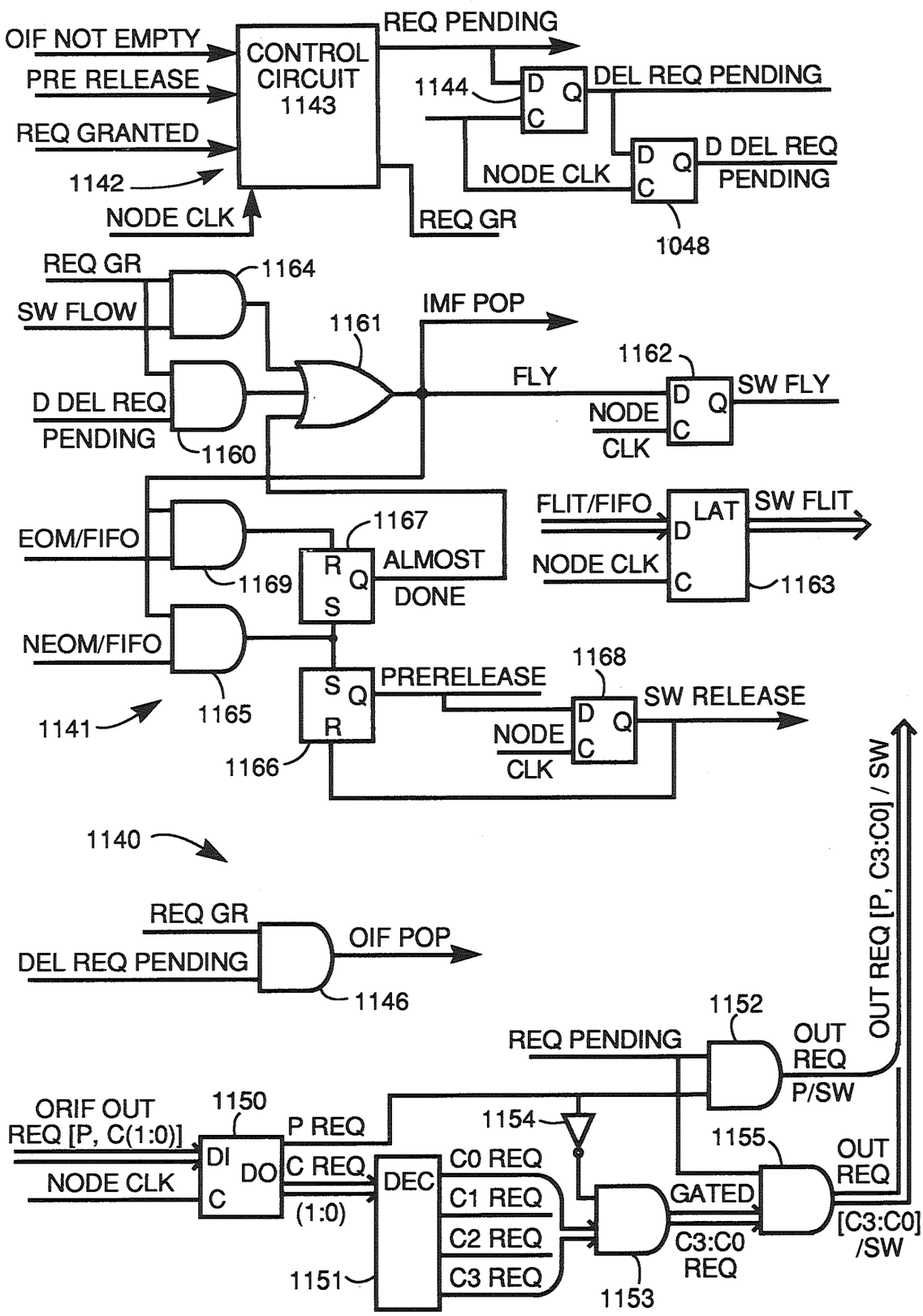

OIF NOT EMPTY
PRE RELEASE
REQ GRANTED
1142
NODE CLK
CONTROL CIRCUIT 1143
REQ PENDING
1144
D
C
Q
DEL REQ PENDING
NODE CLK
D DEL REQ PENDING
1048
REQ GR
1164
SW FLOW
1161
IMF POP
D DEL REQ PENDING
1160
FLY
1162
NODE CLK
SW FLY
EOM/FIFO
1169
1167
R
S
ALMOST DONE
FLIT/FIFO
LAT
SW FLIT
NODE CLK
1163
NEOM/FIFO
1165
1141
S
R
PRERELEASE
1168
SW RELEASE
1166
1140
REQ GR
DEL REQ PENDING
OIF POP
1146
REQ PENDING
1152
OUT REQ P/SW
OUT REQ [P, C3:C0] / SW
ORIF OUT REQ [P, C(1:0)]
1150
DI
C
DO
P REQ
C REQ
(1:0)
NODE CLK
DEC
C0 REQ
C1 REQ
C2 REQ
C3 REQ
1151
1154
GATED
C3:C0 REQ
1153
1155
OUT REQ
[C3:C0] /SW

FIG. 11B-3

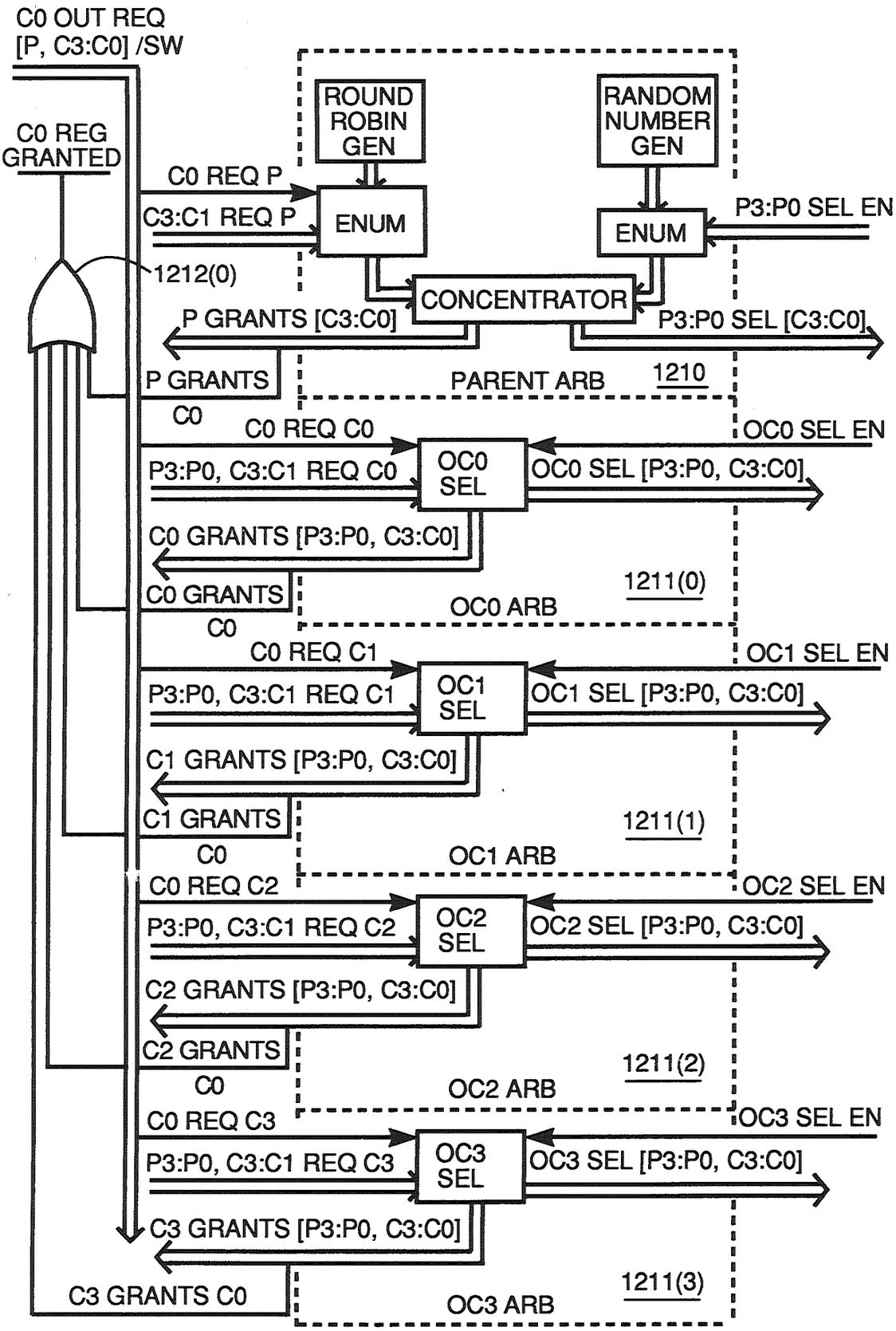

C0 OUT REQ
[P, C3:C0] /SW
C0 REG
GRANTED
ROUND
ROBIN
GEN
RANDOM
NUMBER
GEN
C0 REQ P
C3:C1 REQ P
ENUM
ENUM
P3:P0 SEL EN
1212(0)
CONCENTRATOR
P GRANTS [C3:C0]
P3:P0 SEL [C3:C0]
P GRANTS
PARENT ARB
1210
C0
C0 REQ C0
OC0 SEL EN
P3:P0, C3:C1 REQ C0
OC0
SEL
OC0 SEL [P3:P0, C3:C0]
C0 GRANTS [P3:P0, C3:C0]
C0 GRANTS
1211(0)
OC0 ARB
C0
C0 REQ C1
OC1 SEL EN
P3:P0, C3:C1 REQ C1
OC1
SEL
OC1 SEL [P3:P0, C3:C0]
C1 GRANTS [P3:P0, C3:C0]
C1 GRANTS
1211(1)
C0
OC1 ARB
C0 REQ C2
OC2 SEL EN
P3:P0, C3:C1 REQ C2
OC2
SEL
OC2 SEL [P3:P0, C3:C0]
C2 GRANTS [P3:P0, C3:C0]
C2 GRANTS
1211(2)
C0
OC2 ARB
C0 REQ C3
OC3 SEL EN
P3:P0, C3:C1 REQ C3
OC3
SEL
OC3 SEL [P3:P0, C3:C0]
C3 GRANTS [P3:P0, C3:C0]
C3 GRANTS C0
1211(3)
OC3 ARB

FIG. 11C-1

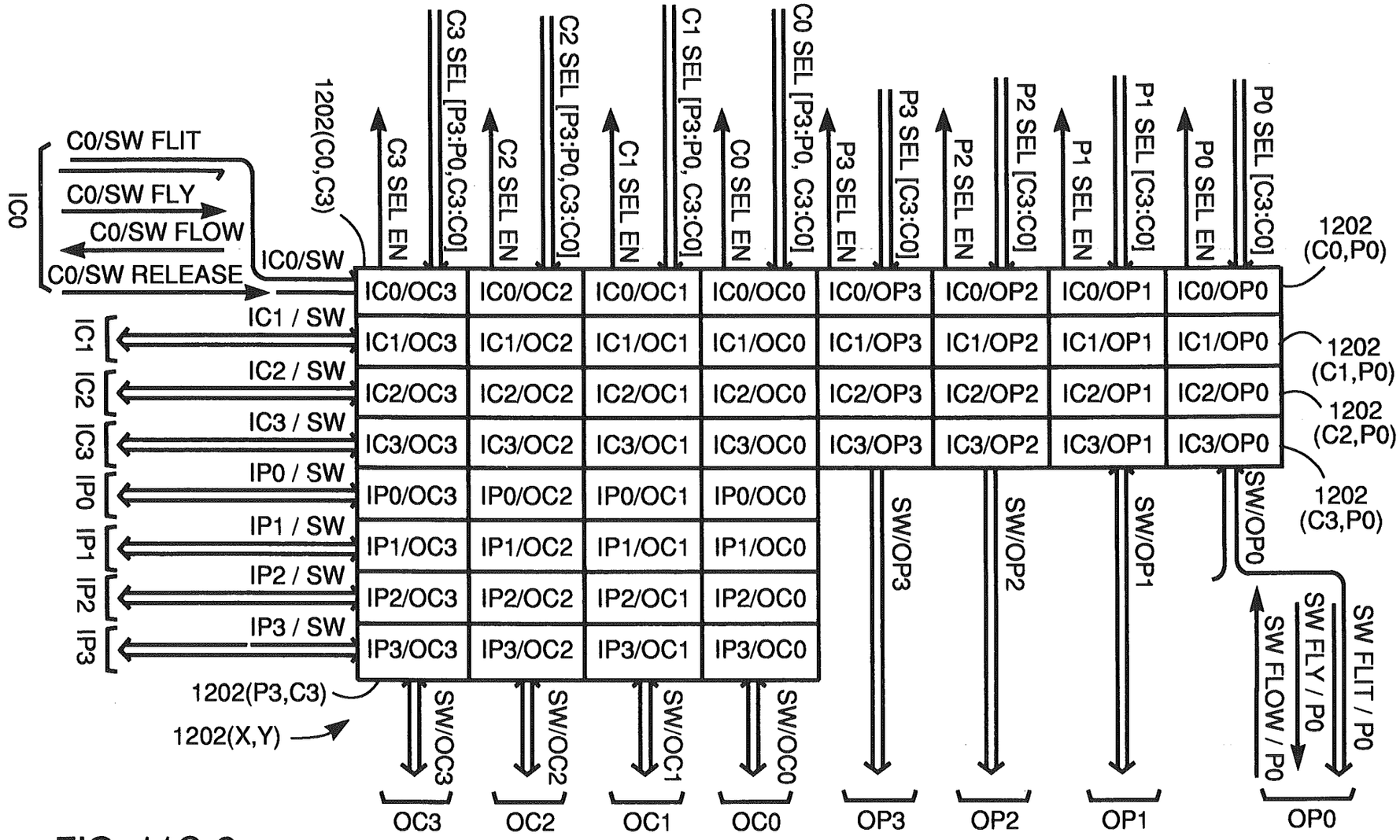

C0/SW FLIT
C0/SW FLY
C0/SW FLOW
C0/SW RELEASE
IC0
IC0/SW
1202(C0,C3)
C3 SEL EN
C3 SEL [P3:P0,C3:C0]
C2 SEL EN
C2 SEL [P3:P0,C3:C0]
C1 SEL EN
C1 SEL [P3:P0, C3:C0]
C0 SEL EN
C0 SEL [P3:P0, C3:C0]
P3 SEL EN
P3 SEL [C3:C0]
P2 SEL EN
P2 SEL [C3:C0]
P1 SEL EN
P1 SEL [C3:C0]
P0 SEL EN
P0 SEL [C3:C0]
1202 (C0,P0)
1202 (C1,P0)
1202 (C2,P0)
1202 (C3,P0)
IC1 / SW
IC2 / SW
IC3 / SW
IP0 / SW
IP1 / SW
IP2 / SW
IP3 / SW
IC1
IC2
IC3
IP0
IP1
IP2
IP3
IC0/OC3 IC0/OC2 IC0/OC1 IC0/OC0 IC0/OP3 IC0/OP2 IC0/OP1 IC0/OP0
IC1/OC3 IC1/OC2 IC1/OC1 IC1/OC0 IC1/OP3 IC1/OP2 IC1/OP1 IC1/OP0
IC2/OC3 IC2/OC2 IC2/OC1 IC2/OC0 IC2/OP3 IC2/OP2 IC2/OP1 IC2/OP0
IC3/OC3 IC3/OC2 IC3/OC1 IC3/OC0 IC3/OP3 IC3/OP2 IC3/OP1 IC3/OP0
IP0/OC3 IP0/OC2 IP0/OC1 IP0/OC0
IP1/OC3 IP1/OC2 IP1/OC1 IP1/OC0
IP2/OC3 IP2/OC2 IP2/OC1 IP2/OC0
IP3/OC3 IP3/OC2 IP3/OC1 IP3/OC0
1202(P3,C3)
1202(X,Y)
SW/OC3
SW/OC2
SW/OC1
SW/OC0
SW/OP3
SW/OP2
SW/OP1
SW/OP0
SW FLIT / P0
SW FLY / P0
SW FLOW / P0
OC3
OC2
OC1
OC0
OP3
OP2
OP1
OP0

FIG. 11C-2

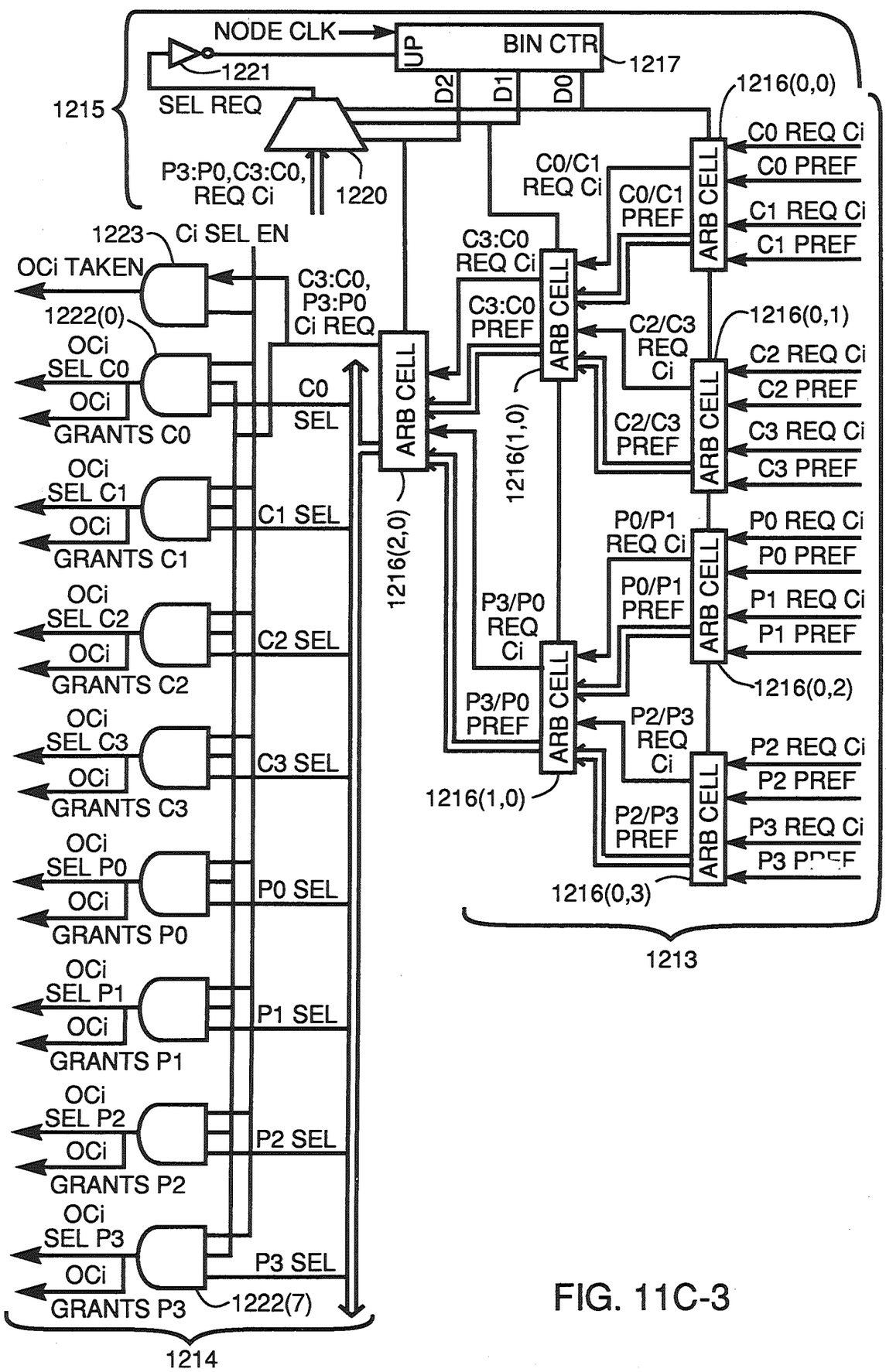

NODE CLK
UP
BIN CTR
1217
1221
D2
D1
D0
1215
SEL REQ
P3:P0,C3:C0,
REQ Ci
1220
1223
Ci SEL EN
OCi TAKEN
C3:C0,
P3:P0
Ci REQ
1222(0)
OCi
SEL C0
OCi
GRANTS C0
C0
SEL
OCi
SEL C1
OCi
GRANTS C1
C1 SEL
OCi
SEL C2
OCi
GRANTS C2
C2 SEL
OCi
SEL C3
OCi
GRANTS C3
C3 SEL
OCi
SEL P0
OCi
GRANTS P0
P0 SEL
OCi
SEL P1
OCi
GRANTS P1
P1 SEL
OCi
SEL P2
OCi
GRANTS P2
P2 SEL
OCi
SEL P3
OCi
GRANTS P3
P3 SEL
1222(7)
1214
ARB CELL
1216(2,0)
1216(1,0)
1216(0,0)
C0 REQ Ci
C0 PREF
C1 REQ Ci
C1 PREF
C0/C1
REQ Ci
C0/C1
PREF
C3:C0
REQ Ci
C3:C0
PREF
1216(0,1)
C2 REQ Ci
C2 PREF
C3 REQ Ci
C3 PREF
C2/C3
REQ
Ci
C2/C3
PREF
P0/P1
REQ Ci
P0 REQ Ci
P0 PREF
P1 REQ Ci
P1 PREF
P0/P1
PREF
P3/P0
REQ
Ci
P3/P0
PREF
1216(0,2)
P2/P3
REQ
Ci
P2 REQ Ci
P2 PREF
P3 REQ Ci
P3 PREF
P2/P3
PREF
1216(0,3)
1213

FIG. 11C-3

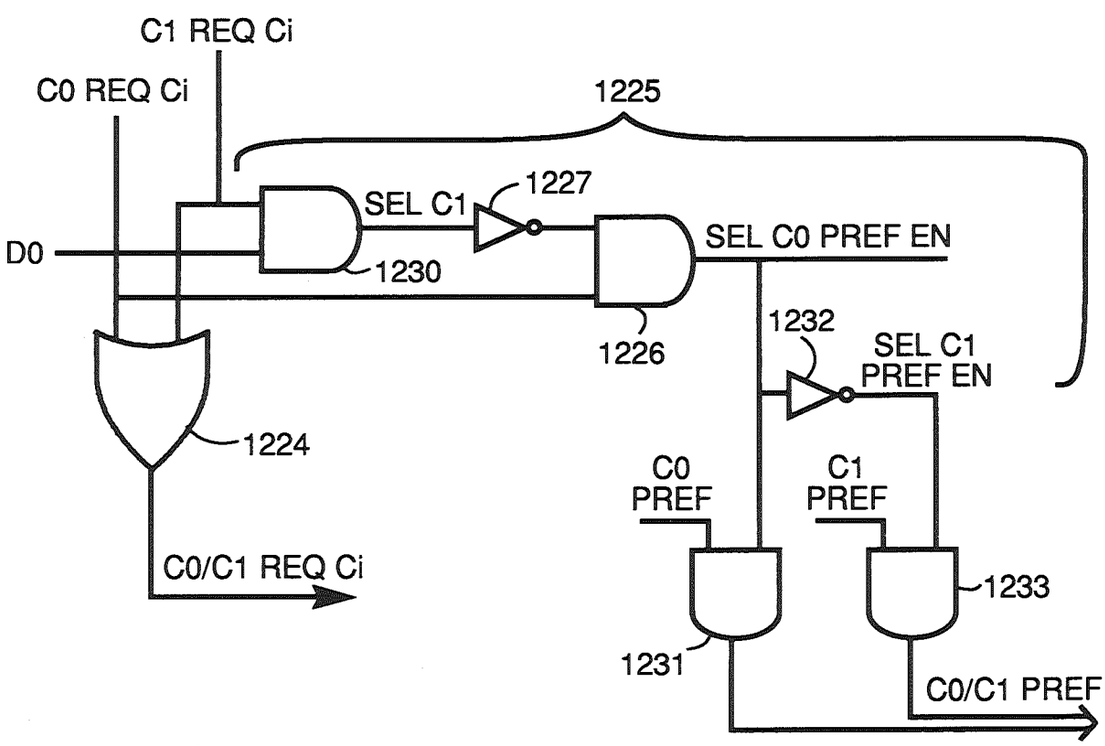

C1 REQ Ci
C0 REQ Ci
1225
SEL C1
1227
D0
1230
SEL C0 PREF EN
1226
1232
SEL C1
PREF EN
1224
C0
PREF
C1
PREF
C0/C1 REQ Ci
1233
1231
C0/C1 PREF

FIG. 11C-4

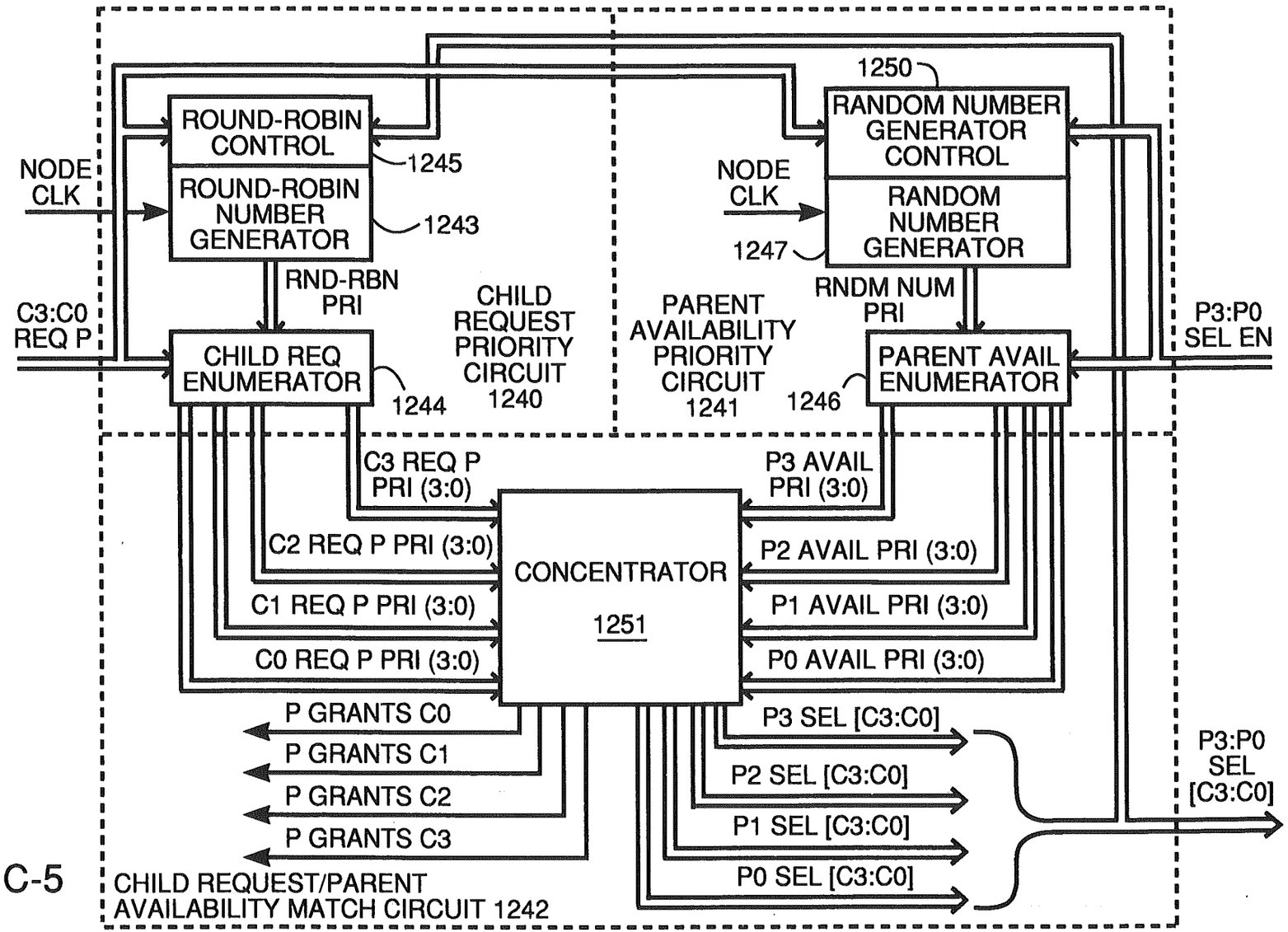
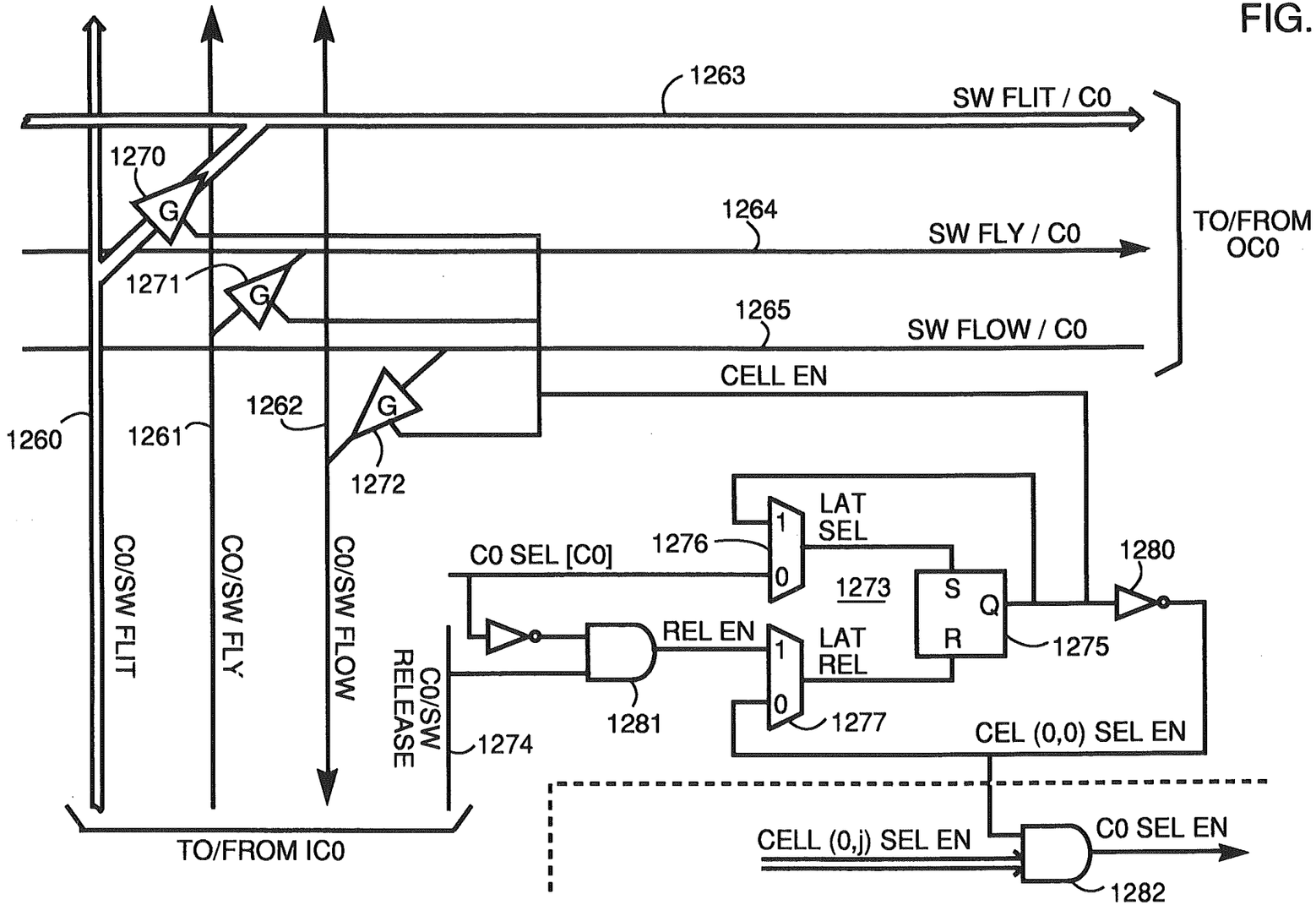

ROUND-ROBIN CONTROL
1245
ROUND-ROBIN NUMBER GENERATOR
1243
NODE CLK
RND-RBN PRI
C3:C0 REQ P
CHILD REQ ENUMERATOR
1244
CHILD REQUEST PRIORITY CIRCUIT 1240
1250
RANDOM NUMBER GENERATOR CONTROL
NODE CLK
RANDOM NUMBER GENERATOR
1247
RNDM NUM PRI
PARENT AVAILABILITY PRIORITY CIRCUIT 1241
P3:P0 SEL EN
PARENT AVAIL ENUMERATOR
1246
C3 REQ P PRI (3:0)
P3 AVAIL PRI (3:0)
C2 REQ P PRI (3:0)
P2 AVAIL PRI (3:0)
CONCENTRATOR
1251
C1 REQ P PRI (3:0)
P1 AVAIL PRI (3:0)
C0 REQ P PRI (3:0)
P0 AVAIL PRI (3:0)
P GRANTS C0
P GRANTS C1
P GRANTS C2
P GRANTS C3
P3 SEL [C3:C0]
P2 SEL [C3:C0]
P1 SEL [C3:C0]
P0 SEL [C3:C0]
P3:P0 SEL [C3:C0]
CHILD REQUEST/PARENT AVAILABILITY MATCH CIRCUIT 1242

FIG. 11C-5

FIG. 11C-6


1263
SW FLIT / C0
1270
G
1264
SW FLY / C0
TO/FROM
OC0
1271
G
1265
SW FLOW / C0
CELL EN
1262
G
1260
1261
1272
LAT
SEL
1276
1
C0 SEL [C0]
0
1280
1273
S
Q
REL EN
LAT
REL
R
1275
1
0
1281
1277
CEL (0,0) SEL EN
C0/SW FLIT
C0/SW FLY
C0/SW FLOW
C0/SW
RELEASE
1274
CELL (0,j) SEL EN
C0 SEL EN
1282
TO/FROM IC0

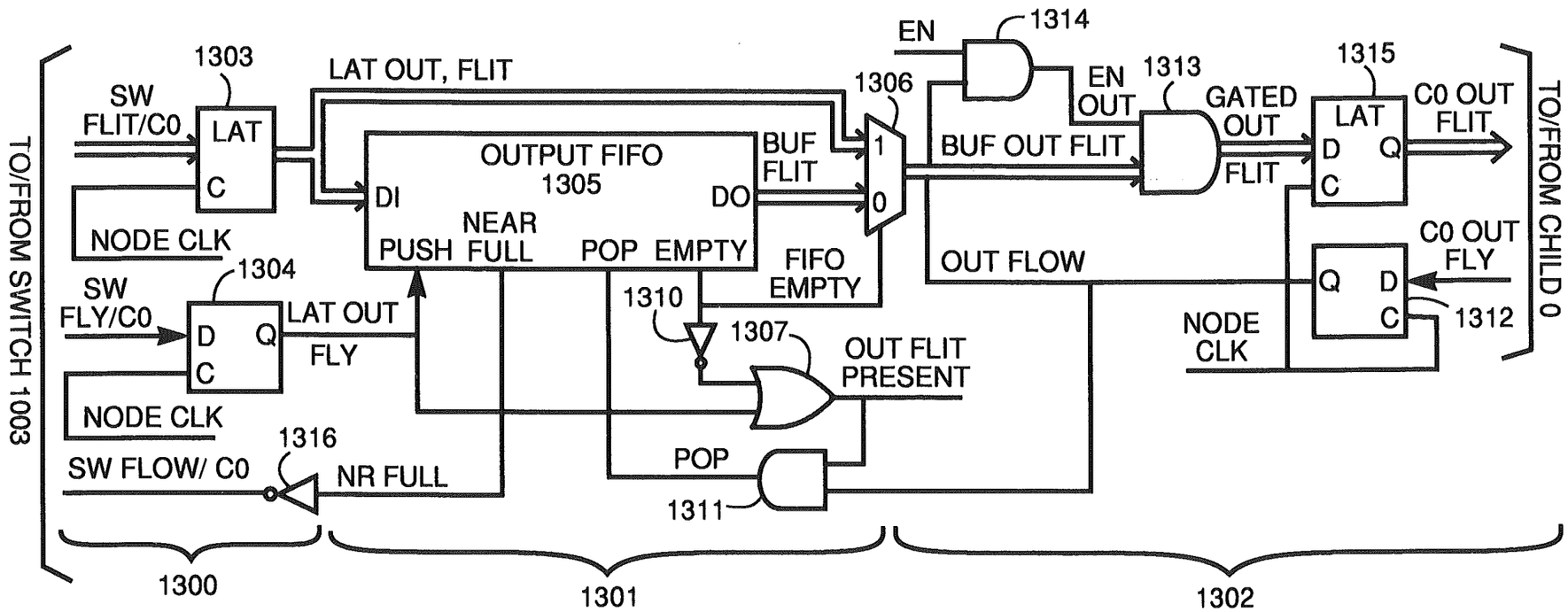

TO/FROM SWITCH 1003
1303
SW
FLIT/C0
LAT
C
NODE CLK
LAT OUT, FLIT
OUTPUT FIFO
1305
DI
DO
NEAR
PUSH FULL
POP EMPTY
BUF
FLIT
1306
1
0
FIFO
EMPTY
1304
SW
FLY/C0
D
Q
C
LAT OUT
FLY
NODE CLK
1316
SW FLOW/ C0
NR FULL
1310
1307
OUT FLIT
PRESENT
POP
1311
EN
1314
EN
OUT
1313
GATED
OUT
FLIT
BUF OUT FLIT
OUT FLOW
1315
LAT
D
Q
C
C0 OUT
FLIT
C0 OUT
FLY
1312
NODE
CLK
TO/FROM CHILD 0
1300
1301
1302

FIG. 11D

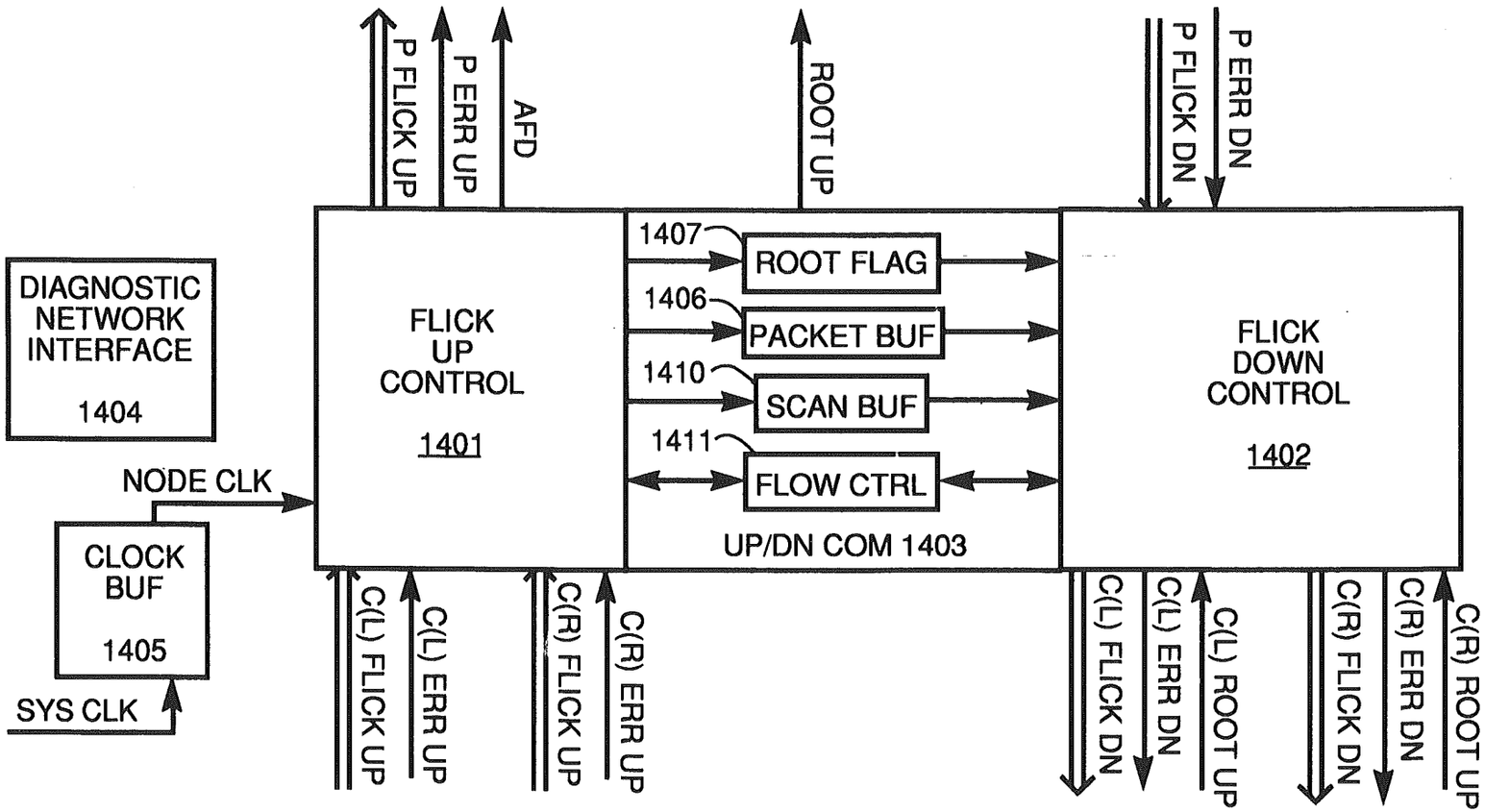

P FLICK UP
P ERR UP
AFD
ROOT UP
P FLICK DN
P ERR DN
DIAGNOSTIC NETWORK INTERFACE
1404
FLICK UP CONTROL
1401
1407
ROOT FLAG
1406
PACKET BUF
1410
SCAN BUF
1411
FLOW CTRL
UP/DN COM 1403
FLICK DOWN CONTROL
1402
NODE CLK
CLOCK BUF
1405
SYS CLK
C(L) FLICK UP
C(L) ERR UP
C(R) FLICK UP
C(R) ERR UP
C(L) FLICK DN
C(L) ERR DN
C(L) ROOT UP
C(R) FLICK DN
C(R) ERR DN
C(R) ROOT UP

FIG. 12A

FIG. 12B

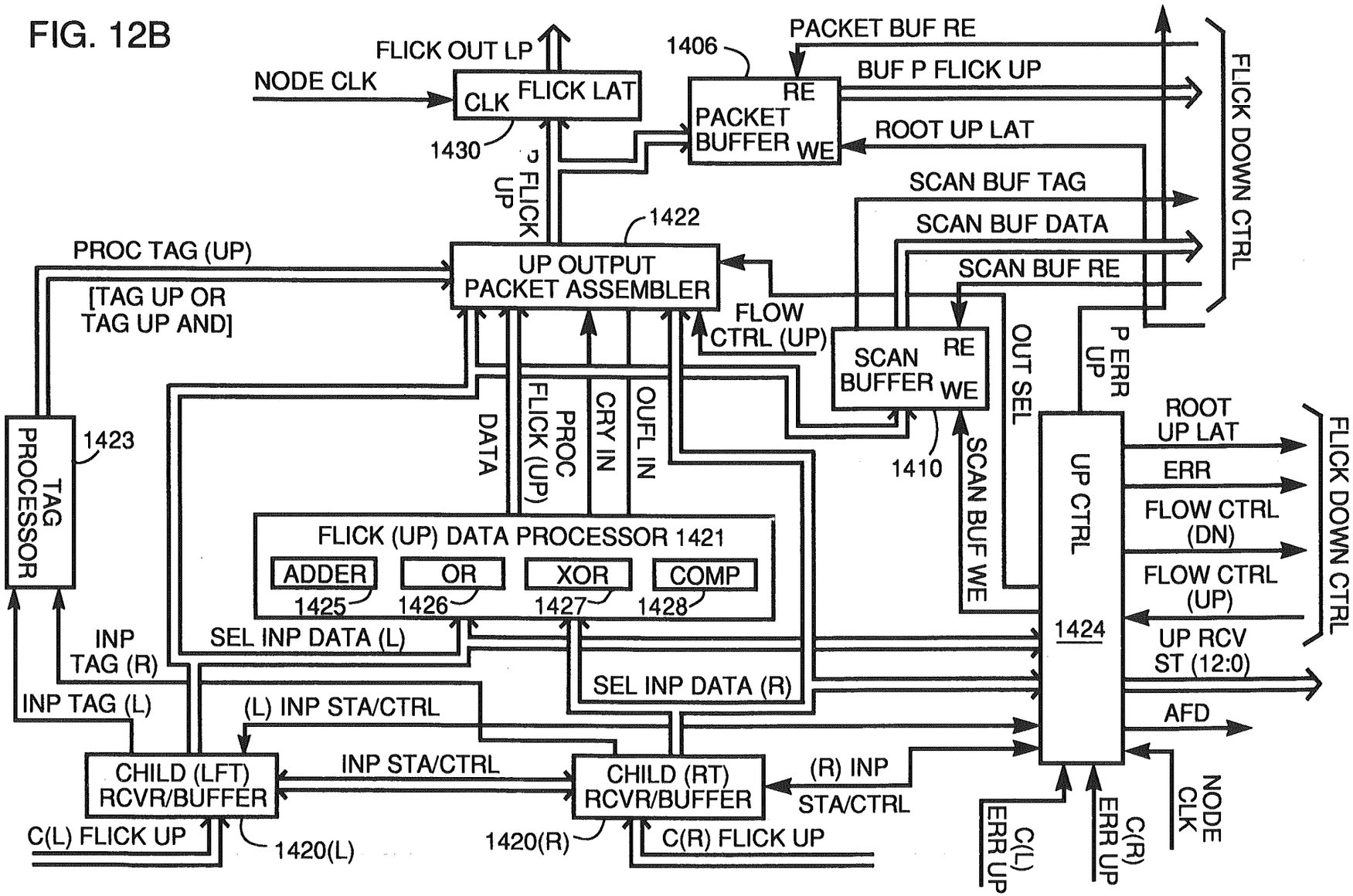

FLICK OUT LP
NODE CLK
CLK
FLICK LAT
1430
P FLICK UP
1406
PACKET BUFFER
RE
WE
PACKET BUF RE
BUF P FLICK UP
ROOT UP LAT
FLICK DOWN CTRL
SCAN BUF TAG
SCAN BUF DATA
SCAN BUF RE
1422
PROC TAG (UP)
[TAG UP OR TAG UP AND]
UP OUTPUT PACKET ASSEMBLER
FLOW CTRL (UP)
SCAN BUFFER
RE
WE
1410
SCAN BUF WE
OUT SEL
P ERR UP
1423
TAG PROCESSOR
DATA
PROC FLICK (UP)
CRY IN
OUFL IN
FLICK (UP) DATA PROCESSOR 1421
ADDER
OR
XOR
COMP
1425
1426
1427
1428
UP CTRL
1424
ROOT UP LAT
ERR
FLOW CTRL (DN)
FLOW CTRL (UP)
UP RCV ST (12:0)
AFD
FLICK DOWN CTRL
SEL INP DATA (L)
SEL INP DATA (R)
INP TAG (R)
INP TAG (L)
(L) INP STA/CTRL
INP STA/CTRL
(R) INP STA/CTRL
CHILD (LFT) RCVR/BUFFER
CHILD (RT) RCVR/BUFFER
C(L) FLICK UP
1420(L)
1420(R)
C(R) FLICK UP
C(L) ERR UP
C(R) ERR UP
NODE CLK

FIG. 12B-1

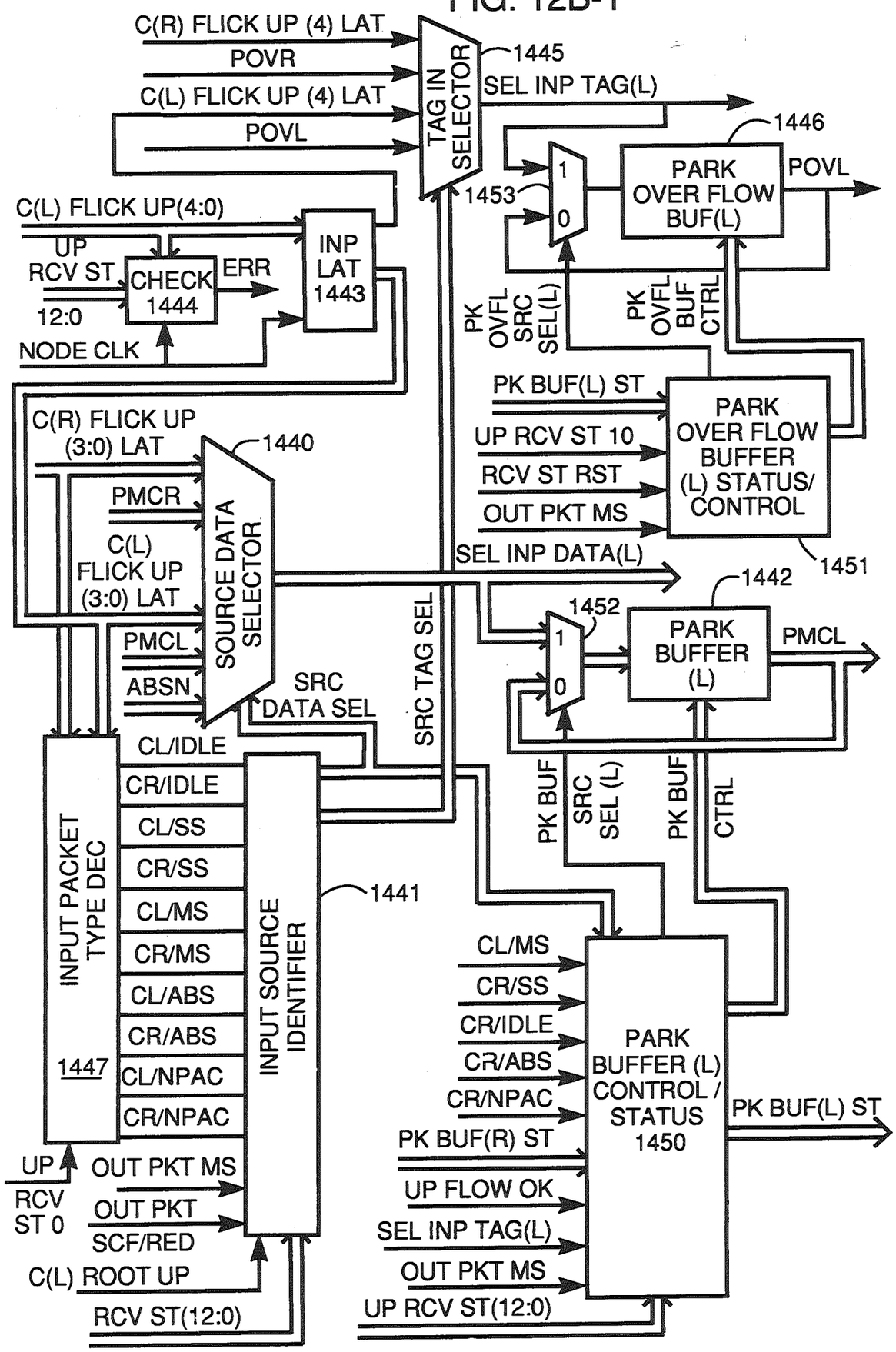

C(R) FLICK UP (4) LAT
POVR
C(L) FLICK UP (4) LAT
POVL
TAG IN SELECTOR
1445
SEL INP TAG(L)
1446
PARK OVER FLOW BUF(L)
POVL
1453
1
0
C(L) FLICK UP(4:0)
UP RCV ST 12:0
CHECK 1444
ERR
INP LAT 1443
NODE CLK
PK OVFL SRC SEL(L)
PK OVFL BUF CTRL
PK BUF(L) ST
UP RCV ST 10
RCV ST RST
OUT PKT MS
PARK OVER FLOW BUFFER (L) STATUS/ CONTROL
1451
C(R) FLICK UP (3:0) LAT
1440
PMCR
C(L) FLICK UP (3:0) LAT
SOURCE DATA SELECTOR
SEL INP DATA(L)
1442
1452
PARK BUFFER (L)
PMCL
PMCL
ABSN
SRC DATA SEL
SRC TAG SEL
CL/IDLE
CR/IDLE
CL/SS
CR/SS
CL/MS
CR/MS
CL/ABS
CR/ABS
CL/NPAC
CR/NPAC
INPUT PACKET TYPE DEC
1447
INPUT SOURCE IDENTIFIER
1441
PK BUF SRC SEL (L)
PK BUF CTRL
CL/MS
CR/SS
CR/IDLE
CR/ABS
CR/NPAC
PK BUF(R) ST
UP FLOW OK
SEL INP TAG(L)
OUT PKT MS
UP RCV ST(12:0)
PARK BUFFER (L) CONTROL / STATUS 1450
PK BUF(L) ST
UP RCV ST 0
OUT PKT MS
OUT PKT SCF/RED
C(L) ROOT UP
RCV ST(12:0)

FIG. 12B-1A

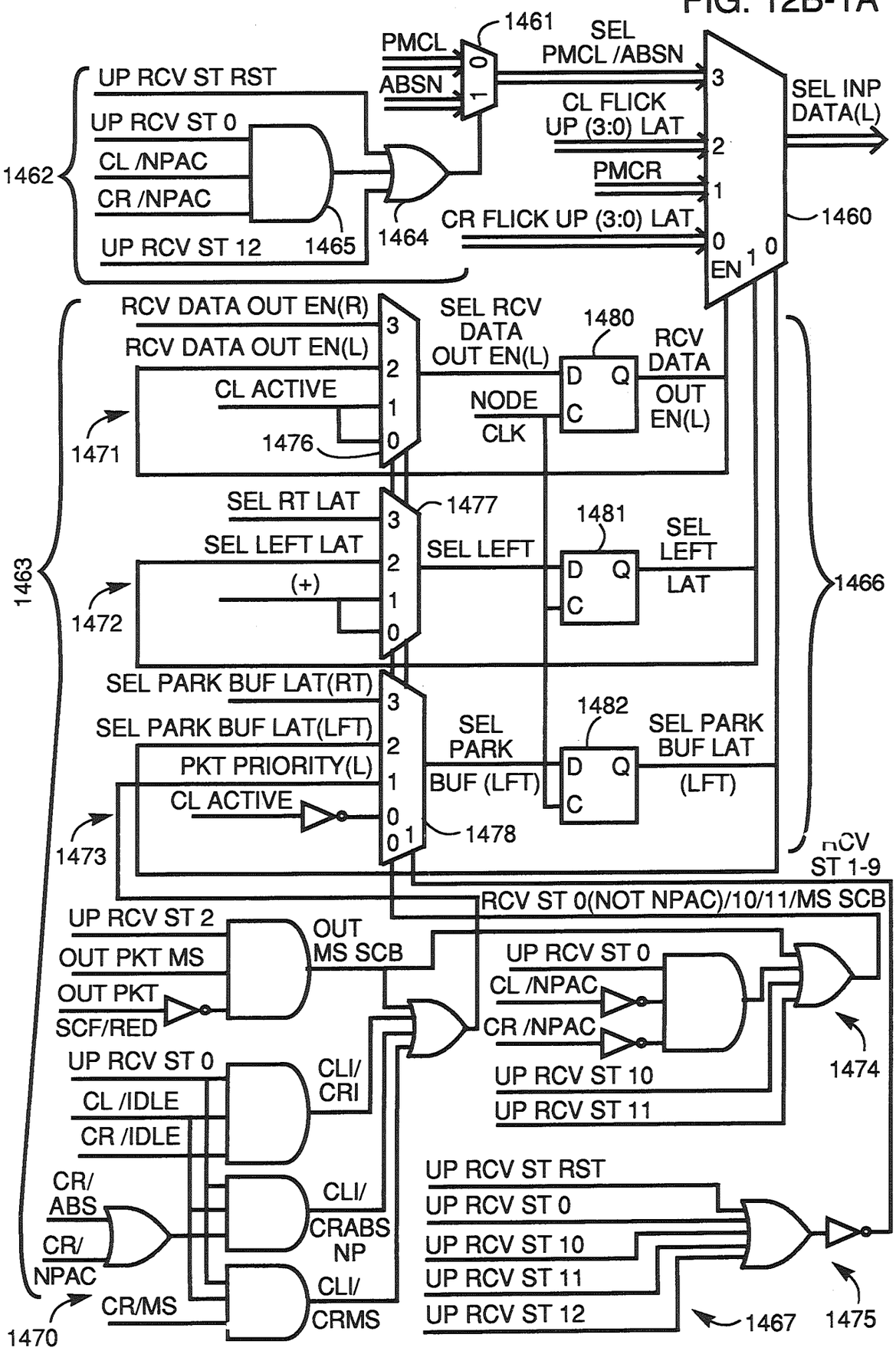

1461
PMCL
ABSN
SEL PMCL /ABSN
SEL INP DATA(L)
CL FLICK UP (3:0) LAT
PMCR
CR FLICK UP (3:0) LAT
1460
UP RCV ST RST
UP RCV ST 0
CL /NPAC
CR /NPAC
UP RCV ST 12
1465
1464
1462
EN
RCV DATA OUT EN(R)
RCV DATA OUT EN(L)
CL ACTIVE
1476
1471
SEL RCV DATA OUT EN(L)
NODE CLK
1480
RCV DATA OUT EN(L)
SEL RT LAT
SEL LEFT LAT
(+)
1472
1477
SEL LEFT
1481
SEL LEFT LAT
1466
1463
SEL PARK BUF LAT(RT)
SEL PARK BUF LAT(LFT)
PKT PRIORITY(L)
CL ACTIVE
1473
1478
SEL PARK BUF (LFT)
1482
SEL PARK BUF LAT (LFT)
RCV ST 1-9
RCV ST 0(NOT NPAC)/10/11/MS SCB
UP RCV ST 2
OUT PKT MS
OUT PKT SCF/RED
OUT MS SCB
UP RCV ST 0
CL /NPAC
CR /NPAC
UP RCV ST 10
UP RCV ST 11
1474
UP RCV ST 0
CL /IDLE
CR /IDLE
CLI/ CRI
CR/ ABS
CR/ NPAC
CLI/ CRABS NP
CR/MS
CLI/ CRMS
1470
UP RCV ST RST
UP RCV ST 0
UP RCV ST 10
UP RCV ST 11
UP RCV ST 12
1467
1475

FIG. 12B-1B

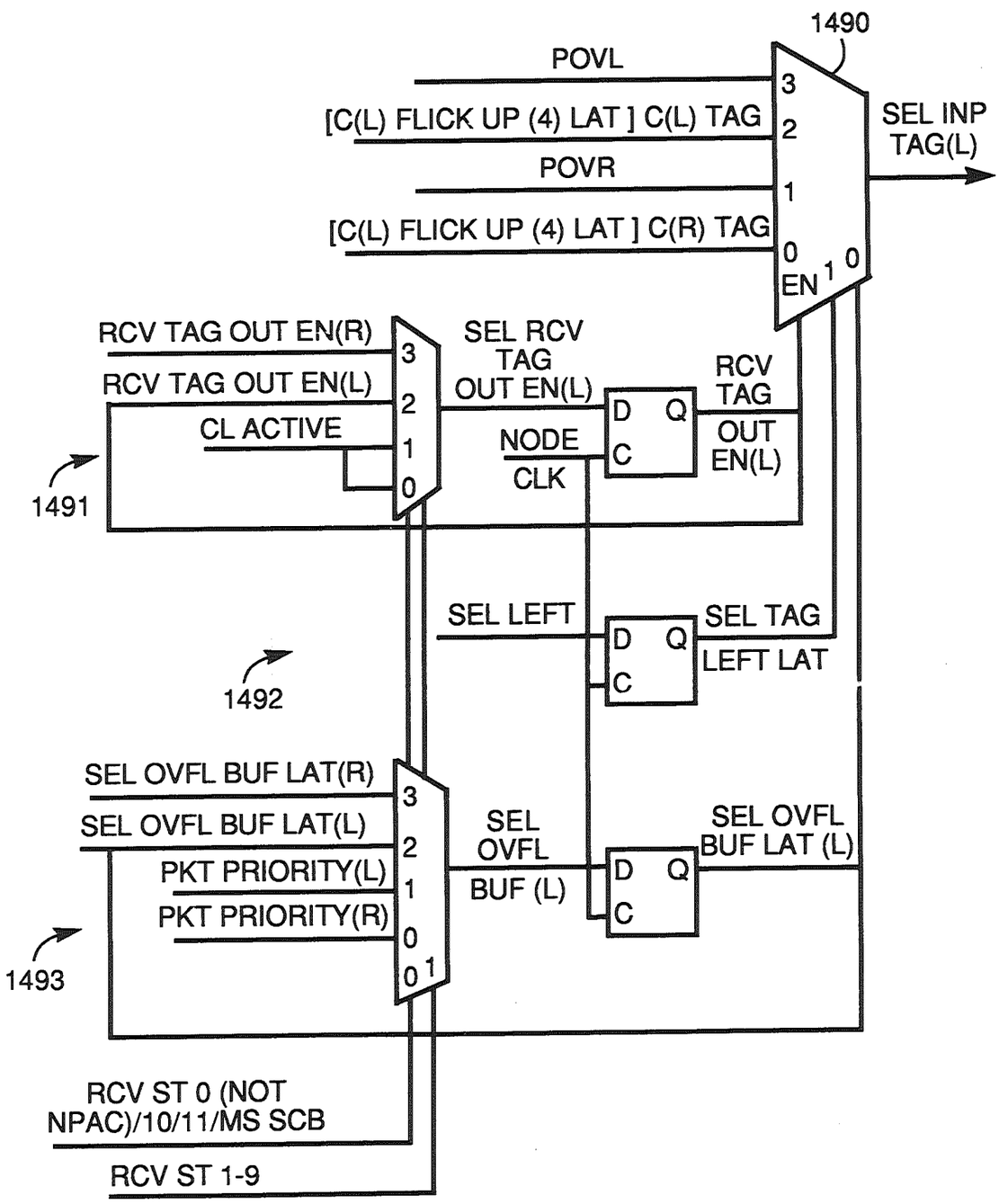

1490
POVL
[C(L) FLICK UP (4) LAT] C(L) TAG
POVR
[C(L) FLICK UP (4) LAT] C(R) TAG
3
2
1
0
EN 1 0
SEL INP TAG(L)
RCV TAG OUT EN(R)
RCV TAG OUT EN(L)
CL ACTIVE
1491
SEL RCV TAG OUT EN(L)
NODE CLK
D Q
C
RCV TAG OUT EN(L)
SEL LEFT
SEL TAG LEFT LAT
1492
SEL OVFL BUF LAT(R)
SEL OVFL BUF LAT(L)
PKT PRIORITY(L)
PKT PRIORITY(R)
1493
SEL OVFL BUF (L)
SEL OVFL BUF LAT (L)
RCV ST 0 (NOT NPAC)/10/11/MS SCB
RCV ST 1-9

FIG. 12B-1C

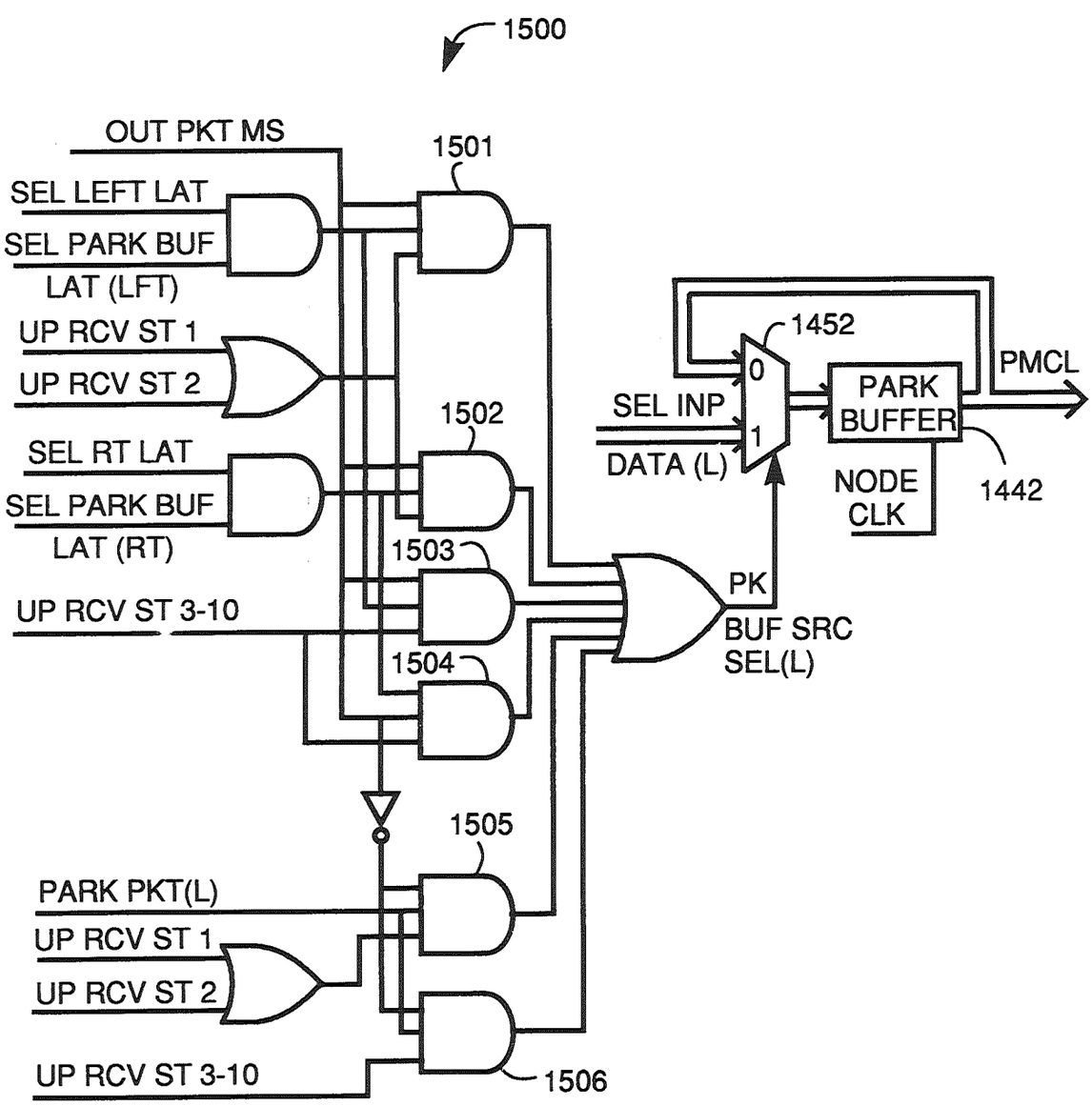
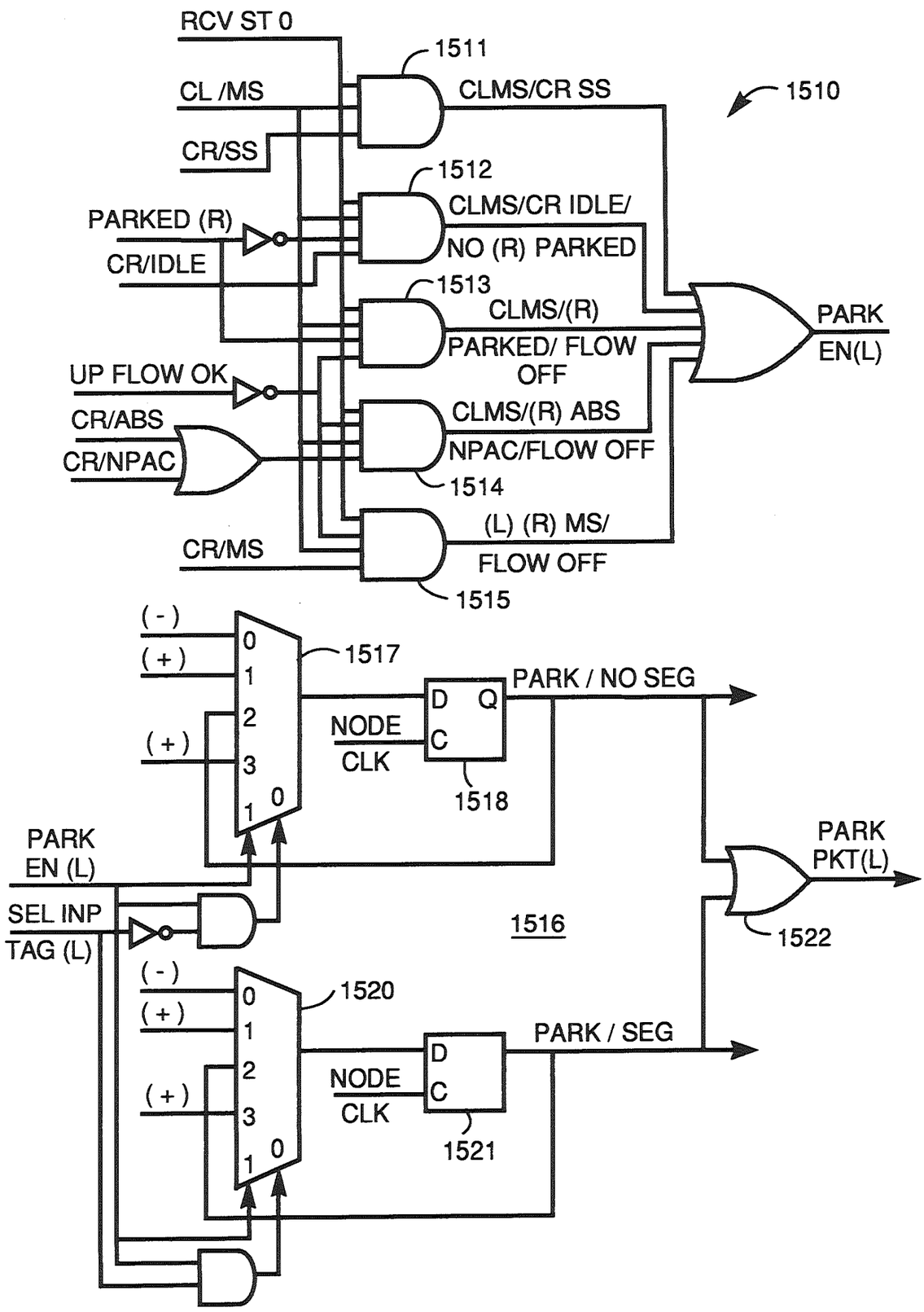

1500
OUT PKT MS
1501
SEL LEFT LAT
SEL PARK BUF
LAT (LFT)
UP RCV ST 1
UP RCV ST 2
1502
SEL RT LAT
SEL PARK BUF
LAT (RT)
1503
UP RCV ST 3-10
1504
1505
PARK PKT(L)
UP RCV ST 1
UP RCV ST 2
UP RCV ST 3-10
1506
1452
0
SEL INP
1
DATA (L)
PARK
BUFFER
PMCL
NODE
CLK
1442
PK
BUF SRC
SEL(L)

FIG. 12B-1D


RCV ST 0
CL /MS
CR/SS
1511
CLMS/CR SS
1510
1512
CLMS/CR IDLE/
NO (R) PARKED
PARKED (R)
CR/IDLE
1513
CLMS/(R)
PARKED/ FLOW
OFF
PARK
EN(L)
UP FLOW OK
CR/ABS
CR/NPAC
CLMS/(R) ABS
NPAC/FLOW OFF
1514
(L) (R) MS/
FLOW OFF
CR/MS
1515
(-)
(+)
(+)
0
1
2
3
1
0
1517
D
Q
C
NODE
CLK
1518
PARK / NO SEG
PARK
EN (L)
SEL INP
TAG (L)
1516
PARK
PKT(L)
1522
(-)
(+)
(+)
0
1
2
3
1
0
1520
D
C
NODE
CLK
1521
PARK / SEG

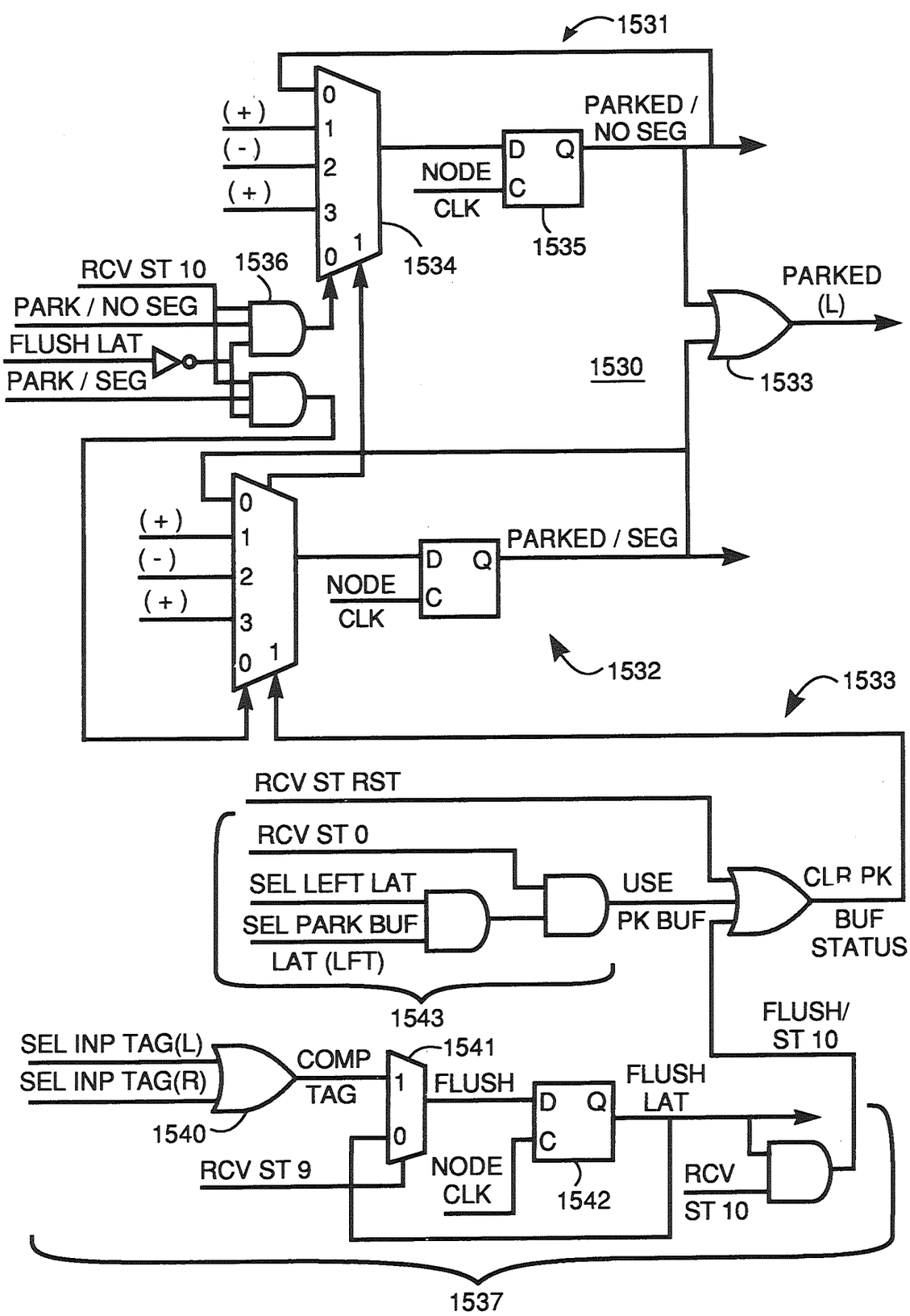

1531
(+)
(-)
(+)
0
1
2
3
0 1
1534
PARKED /
NO SEG
D Q
NODE
CLK
C
1535
RCV ST 10
1536
PARK / NO SEG
FLUSH LAT
PARK / SEG
PARKED
(L)
1530
1533
(+)
(-)
(+)
PARKED / SEG
NODE
CLK
1532
1533
RCV ST RST
RCV ST 0
SEL LEFT LAT
SEL PARK BUF
LAT (LFT)
USE
PK BUF
CLR PK
BUF
STATUS
1543
FLUSH/
ST 10
SEL INP TAG(L)
SEL INP TAG(R)
COMP
TAG
1540
1541
FLUSH
FLUSH
LAT
RCV ST 9
NODE
CLK
1542
RCV
ST 10
1537

FIG. 12B-1E

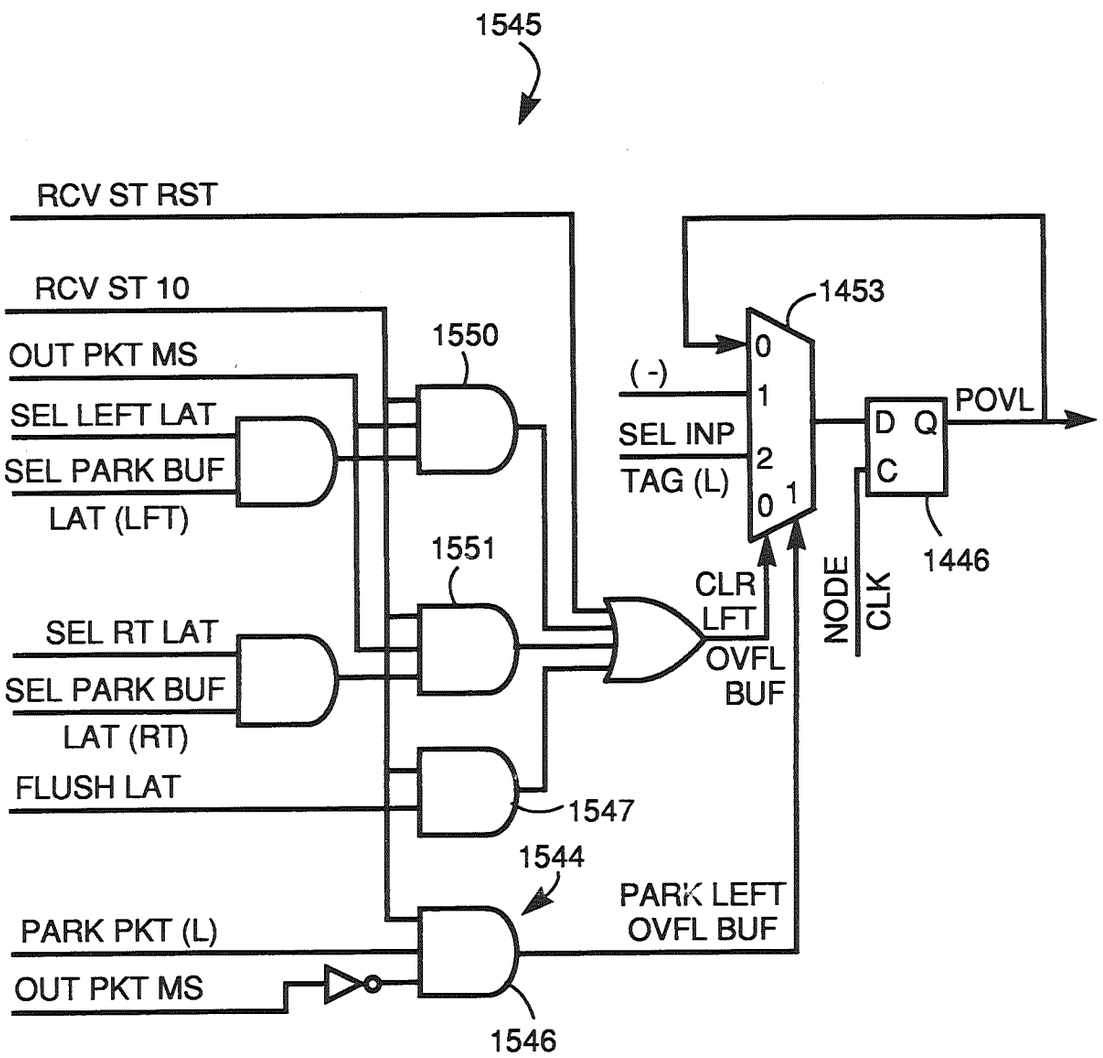

1545
RCV ST RST
RCV ST 10
OUT PKT MS
SEL LEFT LAT
SEL PARK BUF
LAT (LFT)
SEL RT LAT
SEL PARK BUF
LAT (RT)
FLUSH LAT
PARK PKT (L)
OUT PKT MS
1550
1551
1547
1544
1546
1453
0
1
2
0 1
(-)
SEL INP
TAG (L)
CLR
LFT
OVFL
BUF
PARK LEFT
OVFL BUF
D Q
C
POVL
1446
NODE
CLK

FIG. 12B-1F

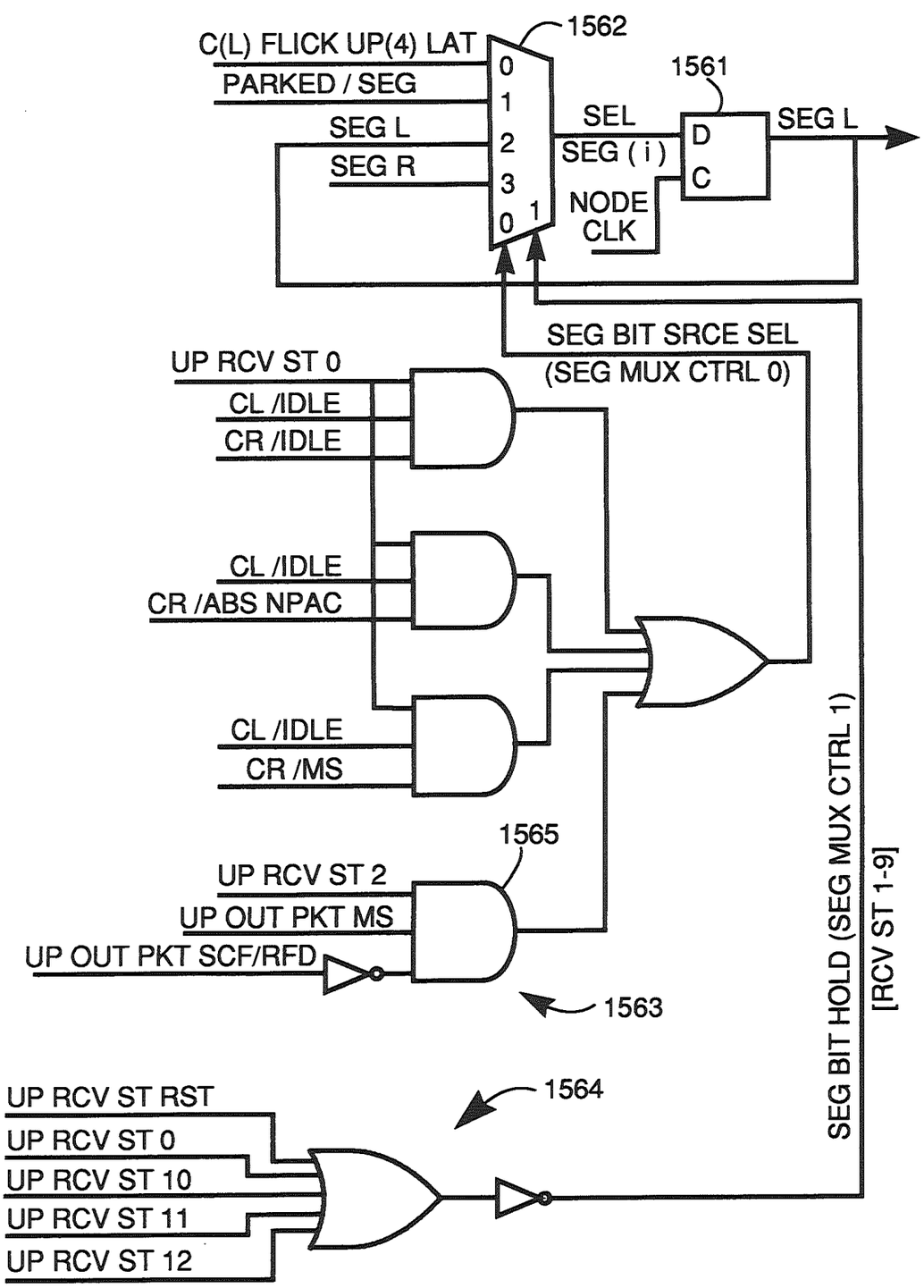

C(L) FLICK UP(4) LAT
PARKED / SEG
SEG L
SEG R
0
1
2
3
0
1
1562
1561
SEL
SEG (i)
NODE CLK
D
C
SEG L
SEG BIT SRCE SEL
(SEG MUX CTRL 0)
UP RCV ST 0
CL /IDLE
CR /IDLE
CL /IDLE
CR /ABS NPAC
CL /IDLE
CR /MS
1565
UP RCV ST 2
UP OUT PKT MS
UP OUT PKT SCF/RFD
1563
1564
UP RCV ST RST
UP RCV ST 0
UP RCV ST 10
UP RCV ST 11
UP RCV ST 12
SEG BIT HOLD (SEG MUX CTRL 1)
[RCV ST 1-9]

FIG. 12B-1G

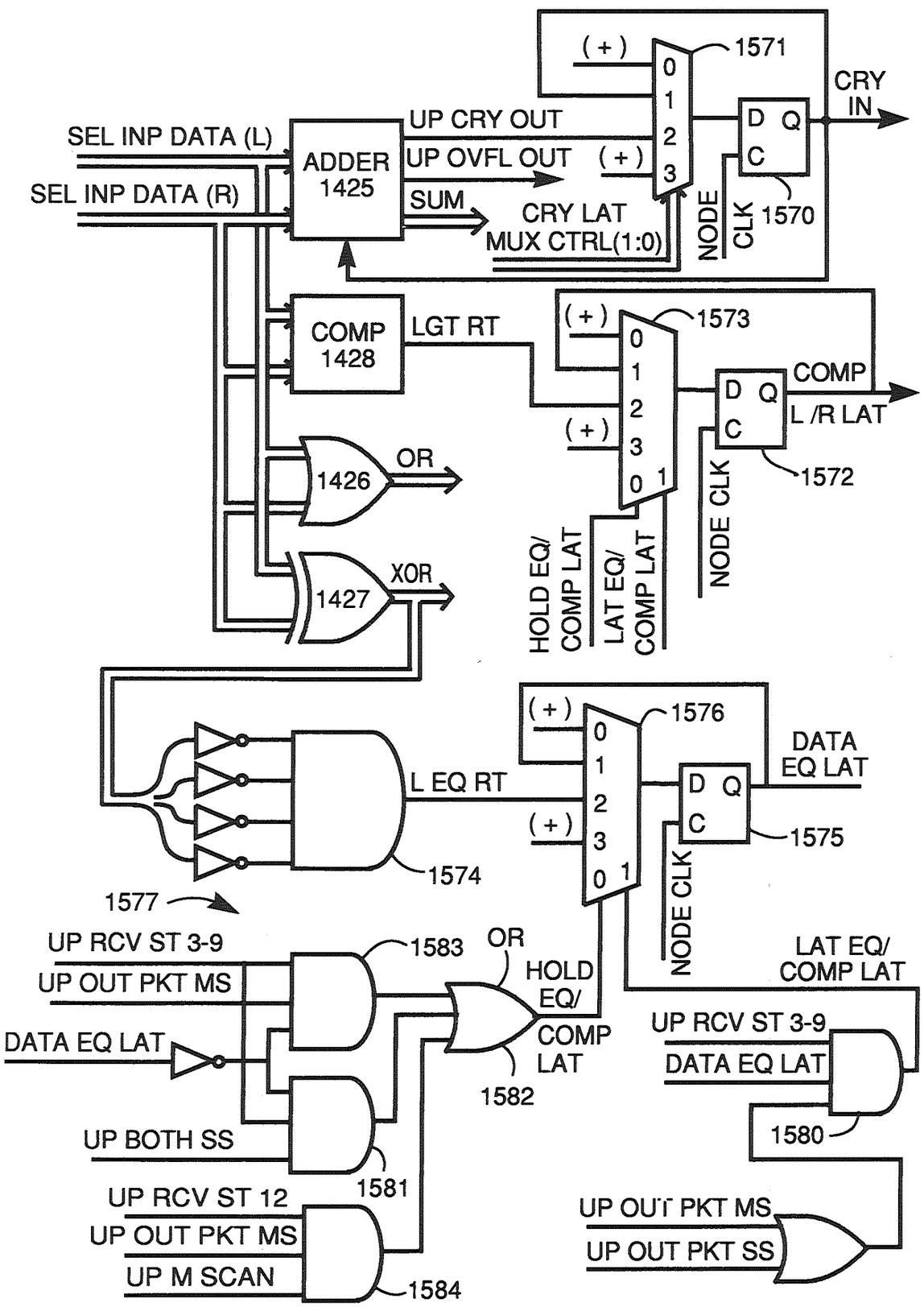

SEL INP DATA (L)
SEL INP DATA (R)
ADDER 1425
UP CRY OUT
UP OVFL OUT
SUM
CRY LAT MUX CTRL(1:0)
(+)
1571
0 1 2 3
D Q
C
CRY IN
NODE CLK
1570
COMP 1428
LGT RT
1573
COMP L /R LAT
1572
1426
OR
1427
XOR
HOLD EQ/ COMP LAT
LAT EQ/ COMP LAT
NODE CLK
L EQ RT
1576
DATA EQ LAT
1575
1574
1577
UP RCV ST 3-9
UP OUT PKT MS
DATA EQ LAT
1583
OR
HOLD EQ/ COMP LAT
1582
UP BOTH SS
1581
UP RCV ST 12
UP OUT PKT MS
UP M SCAN
1584
LAT EQ/ COMP LAT
UP RCV ST 3-9
DATA EQ LAT
1580
UP OUT PKT MS
UP OUT PKT SS

FIG. 12B-2

FIG. 12B-3

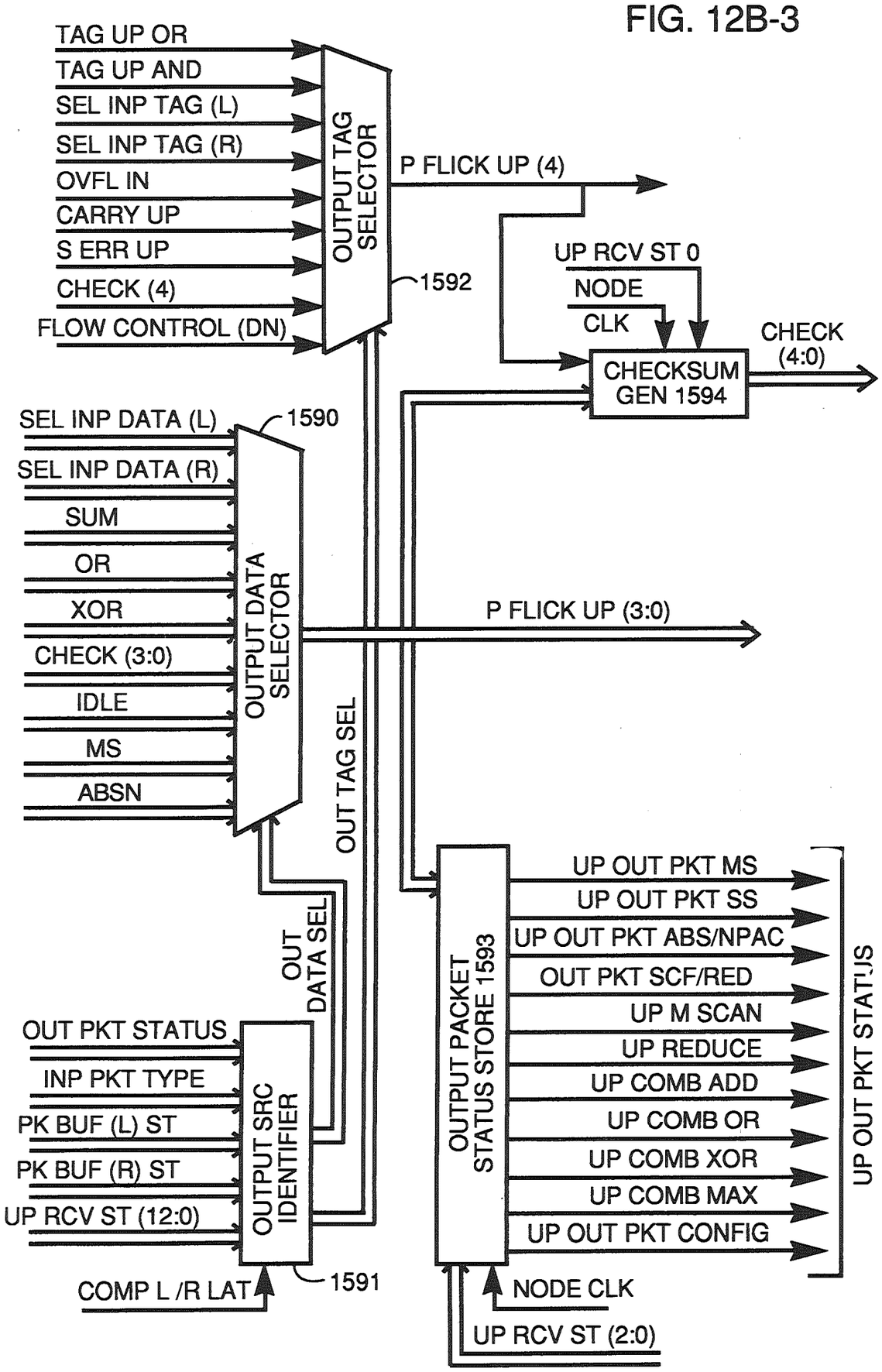
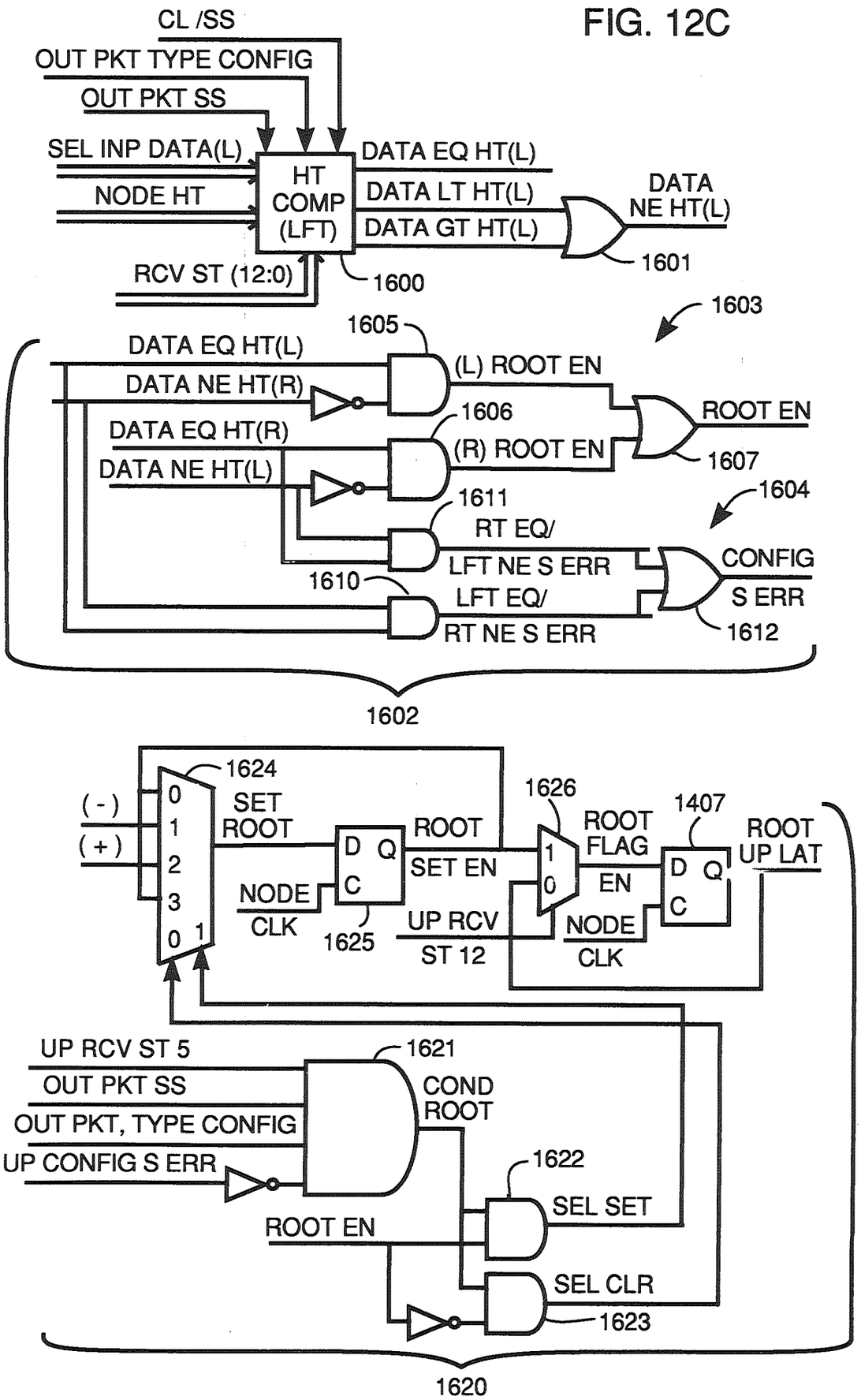

TAG UP OR
TAG UP AND
SEL INP TAG (L)
SEL INP TAG (R)
OVFL IN
CARRY UP
S ERR UP
CHECK (4)
FLOW CONTROL (DN)
OUTPUT TAG SELECTOR
1592
P FLICK UP (4)
UP RCV ST 0
NODE CLK
CHECKSUM GEN 1594
CHECK (4:0)
SEL INP DATA (L)
SEL INP DATA (R)
SUM
OR
XOR
CHECK (3:0)
IDLE
MS
ABSN
1590
OUTPUT DATA SELECTOR
P FLICK UP (3:0)
OUT TAG SEL
OUT DATA SEL
OUT PKT STATUS
INP PKT TYPE
PK BUF (L) ST
PK BUF (R) ST
UP RCV ST (12:0)
OUTPUT SRC IDENTIFIER
1591
COMP L /R LAT
OUTPUT PACKET STATUS STORE 1593
UP OUT PKT MS
UP OUT PKT SS
UP OUT PKT ABS/NPAC
OUT PKT SCF/RED
UP M SCAN
UP REDUCE
UP COMB ADD
UP COMB OR
UP COMB XOR
UP COMB MAX
UP OUT PKT CONFIG
UP OUT PKT STATUS
NODE CLK
UP RCV ST (2:0)

FIG. 12C


CL /SS
OUT PKT TYPE CONFIG
OUT PKT SS
SEL INP DATA(L)
NODE HT
HT COMP (LFT)
DATA EQ HT(L)
DATA LT HT(L)
DATA GT HT(L)
DATA NE HT(L)
1601
RCV ST (12:0)
1600
1603
1605
DATA EQ HT(L)
DATA NE HT(R)
(L) ROOT EN
1606
ROOT EN
DATA EQ HT(R)
DATA NE HT(L)
(R) ROOT EN
1607
1604
1611
RT EQ/
LFT NE S ERR
CONFIG S ERR
1610
LFT EQ/
RT NE S ERR
1612
1602
1624
(-)
(+)
0
1
2
3
0 1
SET ROOT
D Q
C
NODE CLK
1625
ROOT
SET EN
1626
1
0
ROOT FLAG
EN
UP RCV ST 12
1407
D Q
C
NODE CLK
ROOT UP LAT
UP RCV ST 5
OUT PKT SS
OUT PKT, TYPE CONFIG
UP CONFIG S ERR
1621
COND ROOT
1622
SEL SET
ROOT EN
SEL CLR
1623
1620

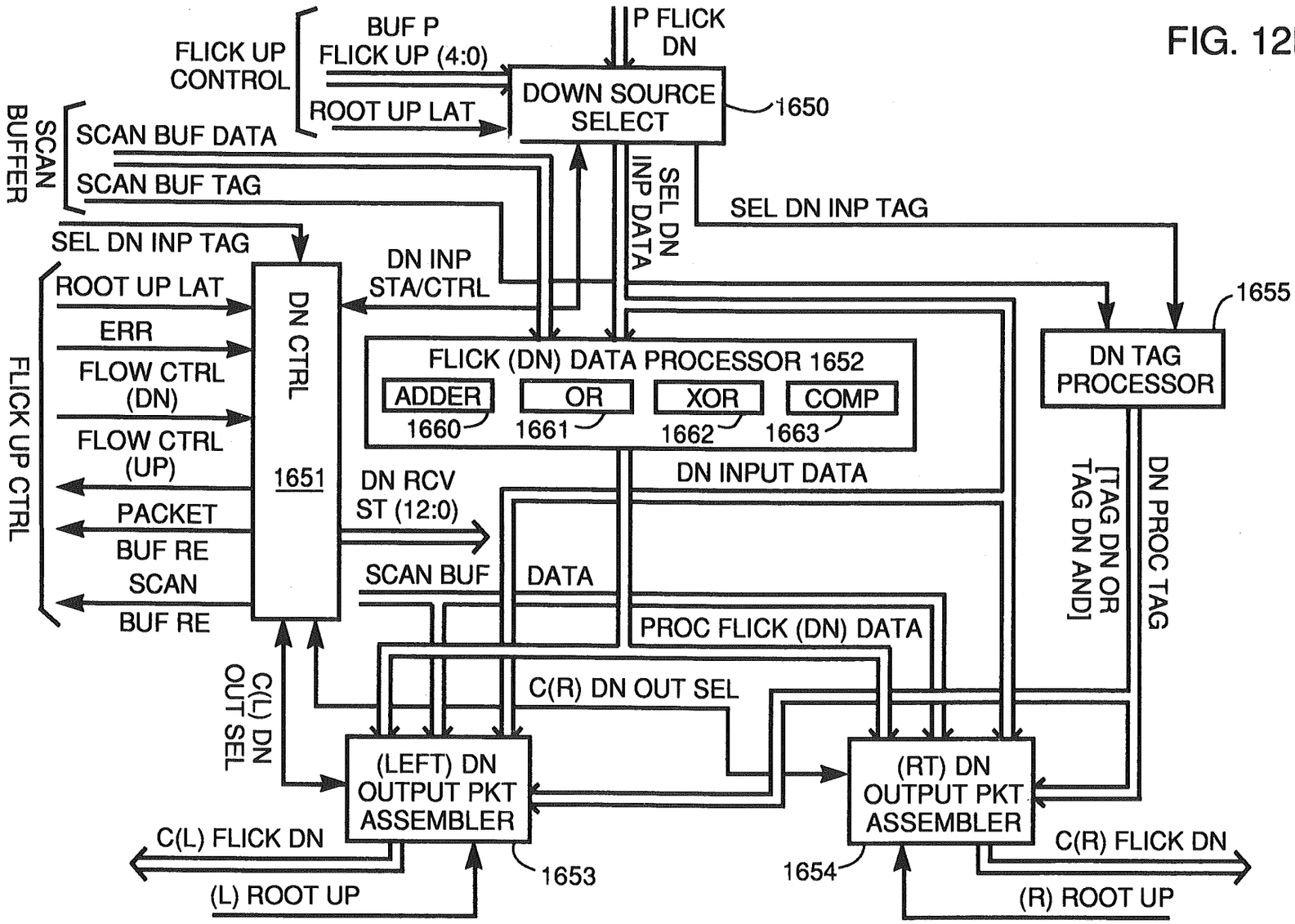

FLICK UP CONTROL
BUF P FLICK UP (4:0)
ROOT UP LAT
P FLICK DN
DOWN SOURCE SELECT
1650
SCAN BUFFER
SCAN BUF DATA
SCAN BUF TAG
SEL DN INP DATA
SEL DN INP TAG
SEL DN INP TAG
DN INP STA/CTRL
1655
ROOT UP LAT
ERR
FLOW CTRL (DN)
FLOW CTRL (UP)
PACKET
BUF RE
SCAN BUF RE
FLICK UP CTRL
DN CTRL
1651
FLICK (DN) DATA PROCESSOR 1652
ADDER
OR
XOR
COMP
1660
1661
1662
1663
DN TAG PROCESSOR
DN INPUT DATA
[TAG DN OR TAG DN AND]
DN PROC TAG
DN RCV ST (12:0)
SCAN BUF
DATA
PROC FLICK (DN) DATA
C(L) DN OUT SEL
C(R) DN OUT SEL
(LEFT) DN OUTPUT PKT ASSEMBLER
(RT) DN OUTPUT PKT ASSEMBLER
C(L) FLICK DN
(L) ROOT UP
1653
1654
C(R) FLICK DN
(R) ROOT UP

FIG. 12D

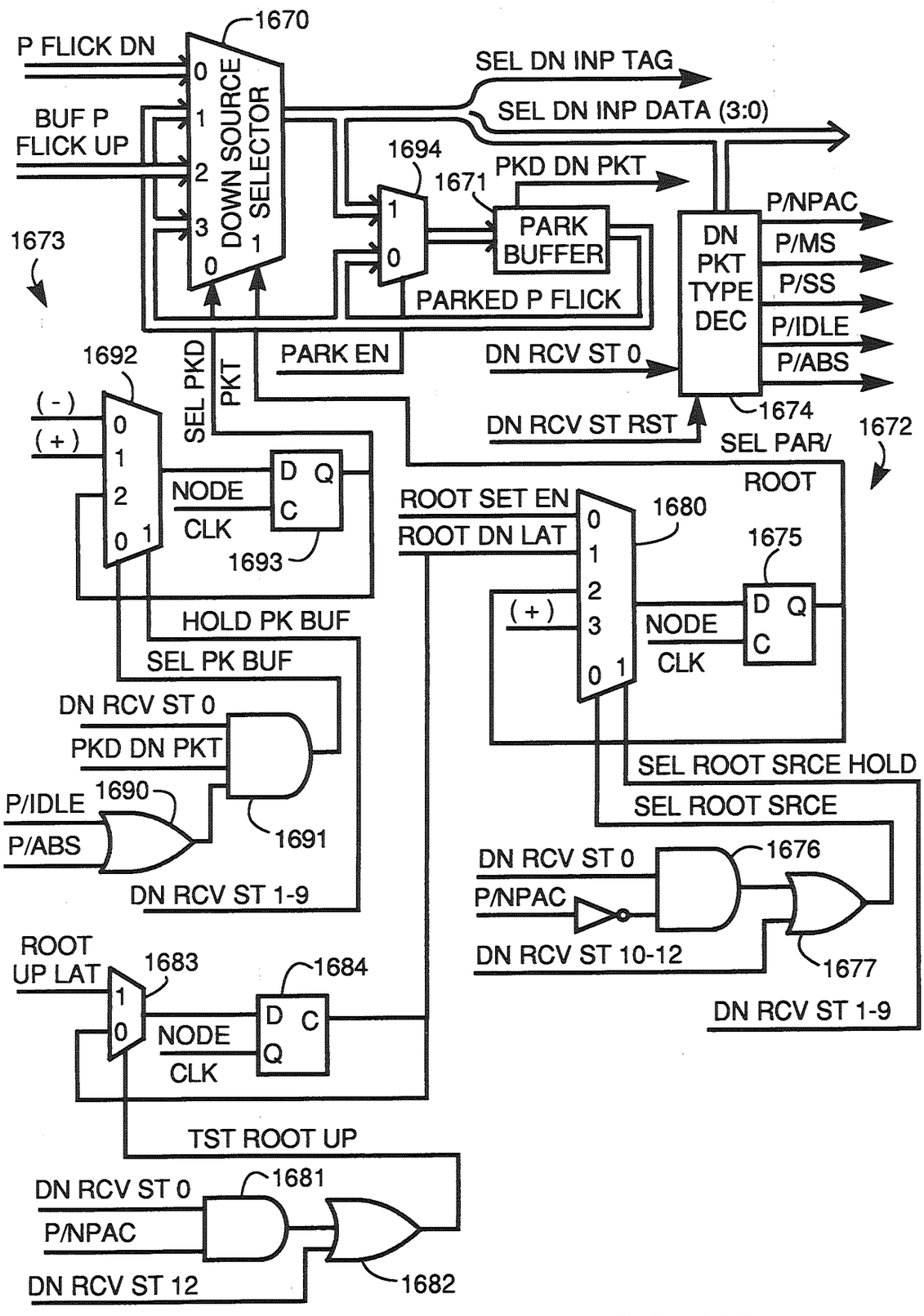

1670
P FLICK DN
BUF P FLICK UP
DOWN SOURCE SELECTOR
0
1
2
3
0
1
SEL DN INP TAG
SEL DN INP DATA (3:0)
1694
1671
PKD DN PKT
PARK BUFFER
PARKED P FLICK
1673
P/NPAC
P/MS
P/SS
P/IDLE
P/ABS
DN PKT TYPE DEC
1674
PARK EN
DN RCV ST 0
DN RCV ST RST
1692
SEL PKD
PKT
(-)
(+)
NODE
CLK
D Q
C
1693
SEL PAR/ ROOT
1672
ROOT SET EN
ROOT DN LAT
1680
1675
HOLD PK BUF
SEL PK BUF
DN RCV ST 0
PKD DN PKT
P/IDLE
P/ABS
1690
1691
DN RCV ST 1-9
SEL ROOT SRCE HOLD
SEL ROOT SRCE
1676
P/NPAC
DN RCV ST 10-12
1677
DN RCV ST 1-9
ROOT UP LAT
1683
1684
TST ROOT UP
1681
1682
DN RCV ST 12

FIG. 12D-1

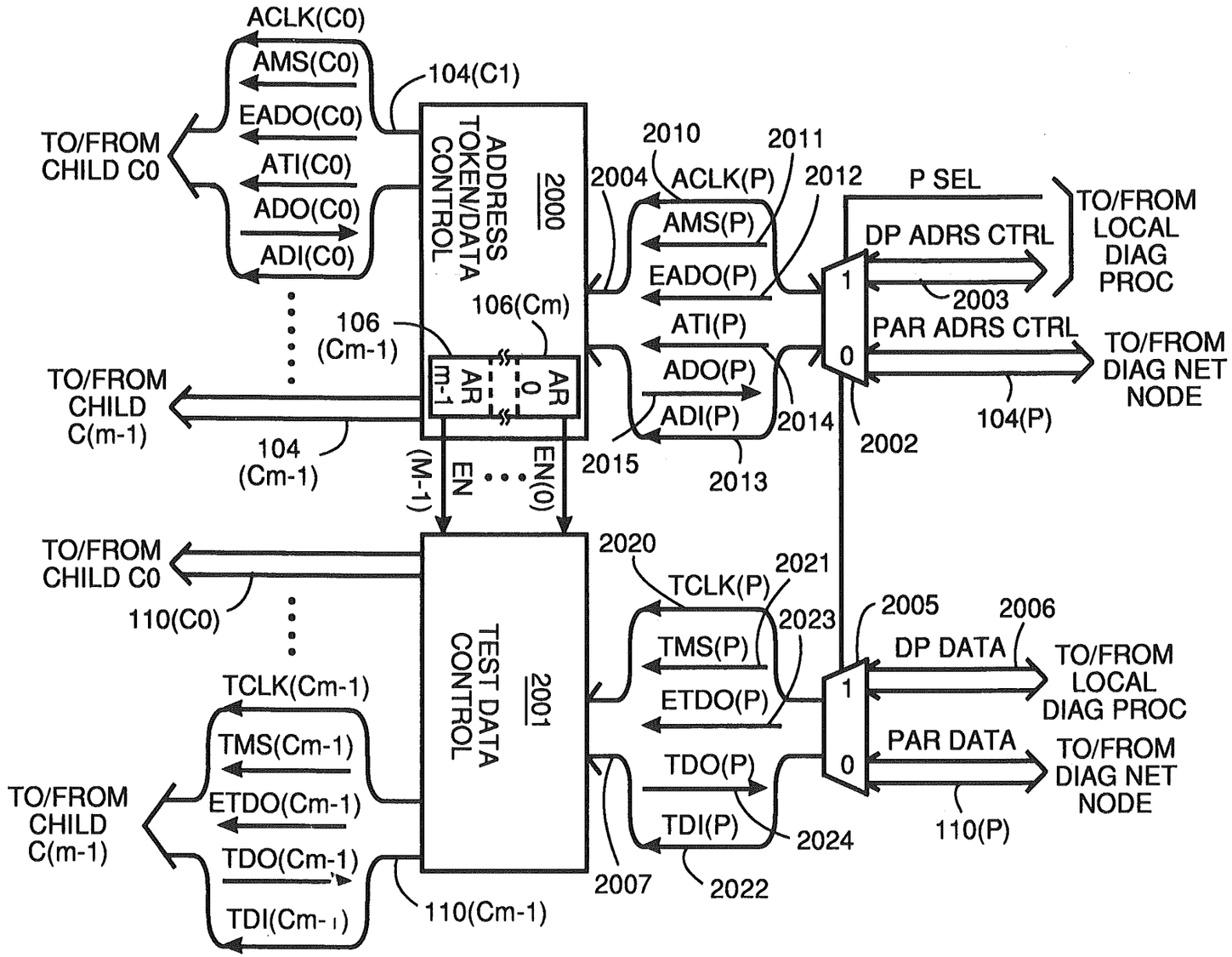

ACLK(C0)
AMS(C0)
EADO(C0)
ATI(C0)
ADO(C0)
ADI(C0)
TO/FROM CHILD C0
104(C1)
ADDRESS TOKEN/DATA CONTROL
2000
106 (Cm-1)
106(Cm)
AR m-1
AR 0
TO/FROM CHILD C(m-1)
104 (Cm-1)
(M-1)
EN
EN(0)
2010
2011
2004
ACLK(P)
2012
AMS(P)
EADO(P)
ATI(P)
ADO(P)
ADI(P)
2015
2014
2013
P SEL
DP ADRS CTRL
2003
PAR ADRS CTRL
TO/FROM LOCAL DIAG PROC
TO/FROM DIAG NET NODE
104(P)
2002
1
0
TO/FROM CHILD C0
110(C0)
TEST DATA CONTROL
2001
2020
2021
TCLK(P)
2023
TMS(P)
ETDO(P)
TDO(P)
TDI(P)
2007
2022
2024
2005
2006
DP DATA
PAR DATA
TO/FROM LOCAL DIAG PROC
TO/FROM DIAG NET NODE
110(P)
TCLK(Cm-1)
TMS(Cm-1)
ETDO(Cm-1)
TDO(Cm-1)
TDI(Cm-1)
TO/FROM CHILD C(m-1)
110(Cm-1)

FIG. 13A

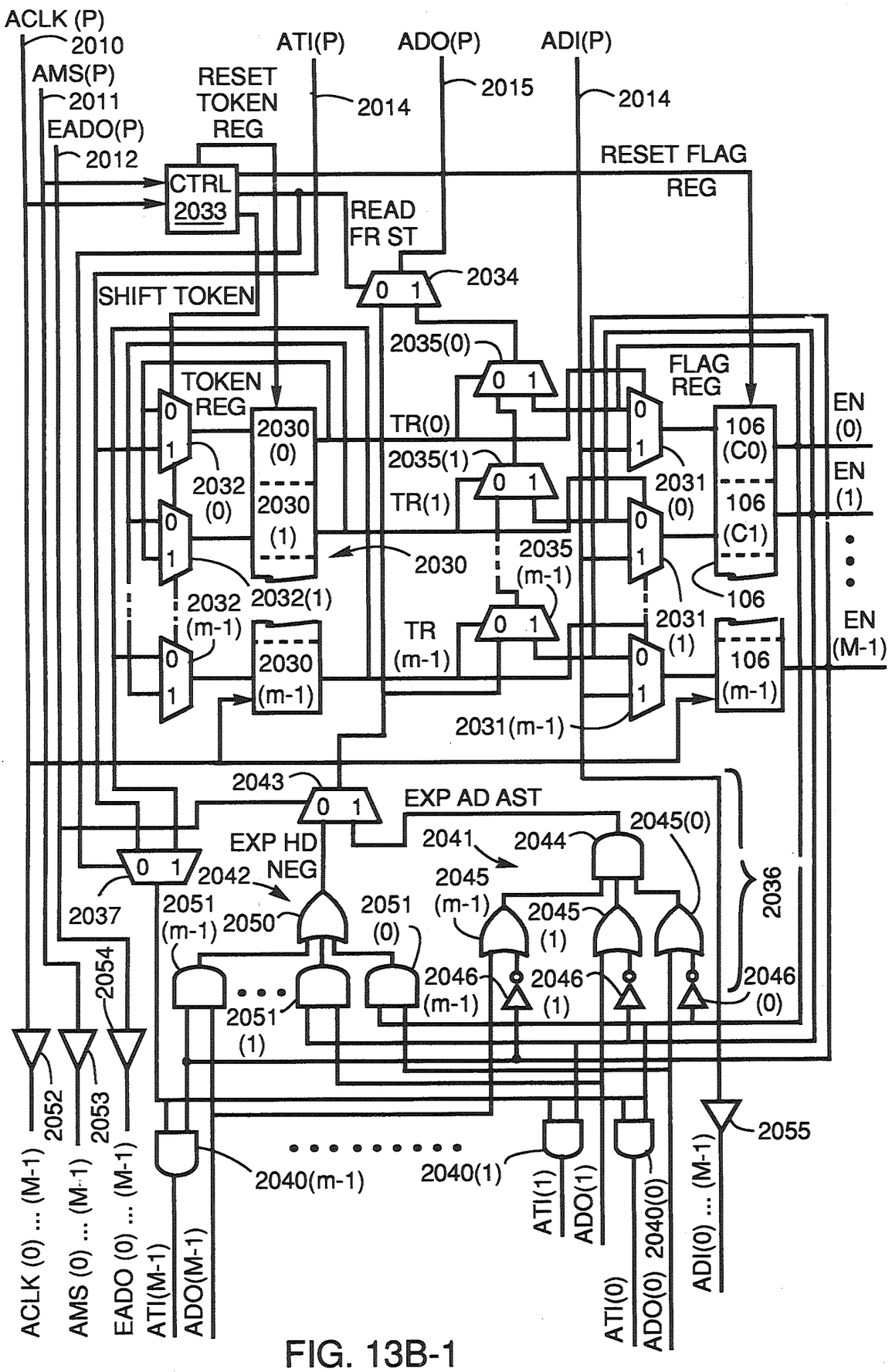
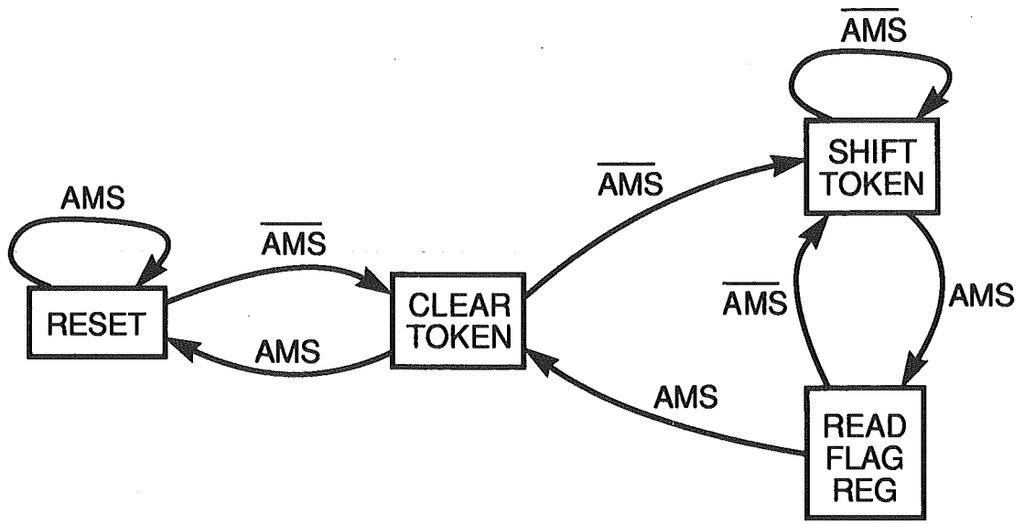

ACLK (P)
2010
AMS(P)
2011
EADO(P)
2012
ATI(P)
ADO(P)
ADI(P)
RESET TOKEN REG
2014
2015
2014
RESET FLAG REG
CTRL 2033
READ FR ST
2034
SHIFT TOKEN
2035(0)
TOKEN REG
FLAG REG
TR(0)
2035(1)
TR(1)
2030 (0)
2030 (1)
2030
2032 (0)
2032(1)
2032 (m-1)
2030 (m-1)
2035 (m-1)
TR (m-1)
2031 (0)
2031 (1)
2031(m-1)
106 (C0)
106 (C1)
106
106 (m-1)
EN (0)
EN (1)
EN (M-1)
2043
EXP AD AST
EXP HD NEG
2042
2037
2041
2044
2045(0)
2045 (m-1)
2045 (1)
2036
2051 (m-1)
2050
2051 (0)
2051 (1)
2046 (m-1)
2046 (1)
2046 (0)
2054
2052
2053
2055
2040(m-1)
2040(1)
ACLK (0) ... (M-1)
AMS (0) ... (M-1)
EADO (0) ... (M-1)
ATI(M-1)
ADO(M-1)
ATI(1)
ADO(1)
ATI(0)
ADO(0)
2040(0)
ADI(0) ... (M-1)

FIG. 13B-1

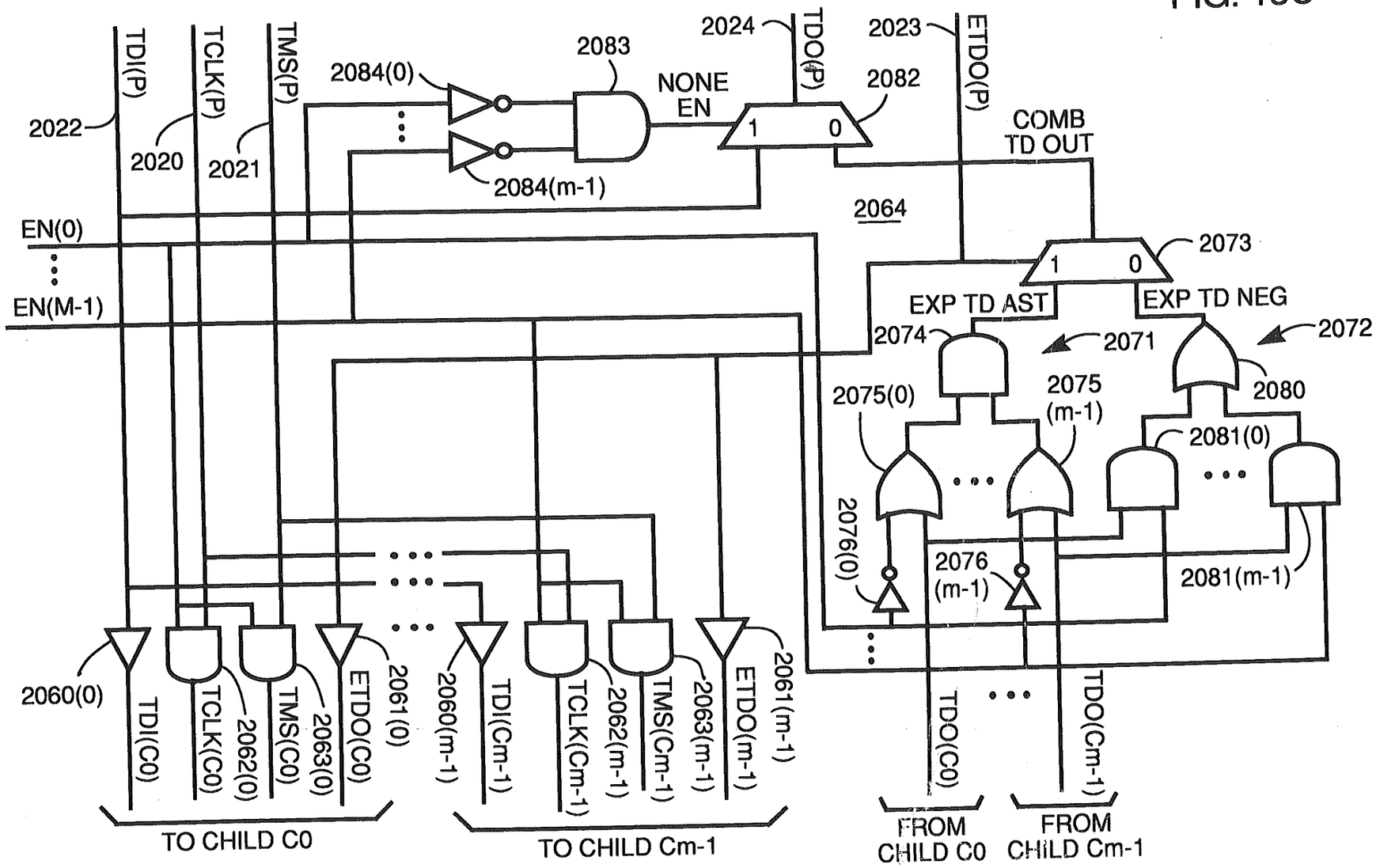
FIG. 13B-2



SIGNAL CONDITION/STATE TABLE

SIGNAL \ STATE	RESET	CLEAR TOKEN	SHIFT TOKEN	READ FLAG REG
RESET TOKEN REG	ASSERT	ASSERT	NEGATE	NEGATE
RESET FLAG REG	ASSERT	NEGATE	NEGATE	NEGATE
READ FR ST	NEGATE	NEGATE	ASSERT	ASSERT
SHIFT TOKEN	NEGATE	NEGATE	ASSERT	NEGATE

FIG. 13C


TDI(P)
TCLK(P)
TMS(P)
2022
2020
2021
2084(0)
2083
NONE EN
2024
TDO(P)
2023
ETDO(P)
2082
1
0
COMB TD OUT
2084(m-1)
2064
EN(0)
EN(M-1)
2073
EXP TD AST
EXP TD NEG
2074
2071
2072
2075(0)
2075 (m-1)
2080
2081(0)
2076(0)
2076 (m-1)
2081(m-1)
2060(0)
TDI(C0)
TCLK(C0)
2062(0)
TMS(C0)
2063(0)
ETDO(C0)
2061(0)
2060(m-1)
TDI(Cm-1)
TCLK(Cm-1)
2062(m-1)
TMS(Cm-1)
2063(m-1)
ETDO(m-1)
2061(m-1)
TDO(C0)
TDO(Cm-1)
TO CHILD C0
TO CHILD Cm-1
FROM CHILD C0
FROM CHILD Cm-1